ADVANTECH

Enabling an Intelligent Planet

MI/O Extension™ Single Board Computer Specification

V2.0
June 2017

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Revision History

Version	Date	Description
V1.0	2011/11/16	
V2.0	2017/6/8	Addendum 2.2 DisplayPort design guideline 2.6 USB 3.0 design guideline

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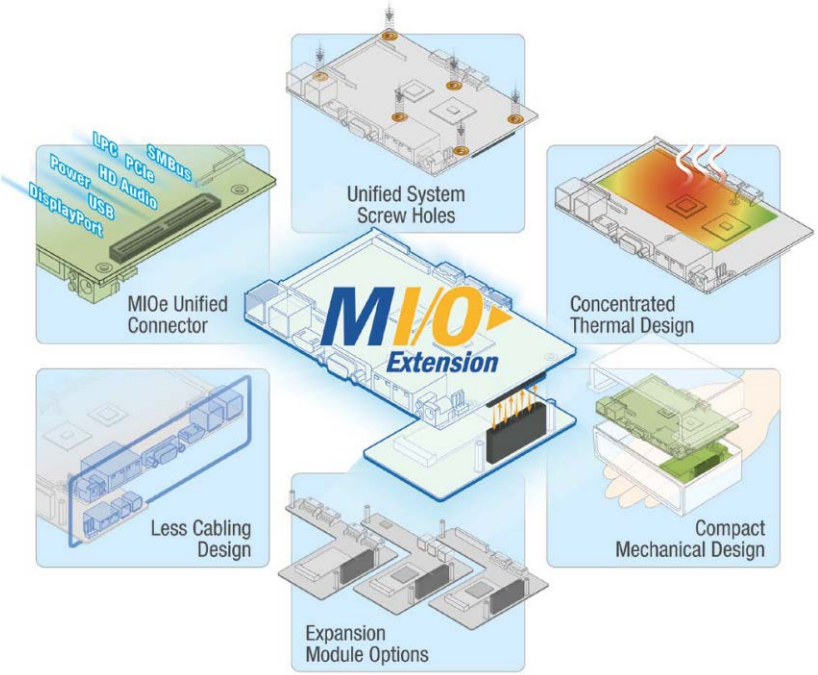
Chapter 1 General Information

1.1 Overview

The innovative MI/O (multiple I/O) Extension Single Board Computer equipped flexible Multiple I/O, efficiency on schedule, development resources & assist integrators to provide optimized solutions in cost-effective way, while still securing the domain knowhow in key vertical industrial technologies.



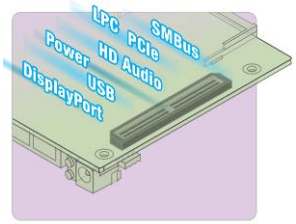
By connecting with MIOe I/O extension modules through high speed sockets, customers get the most flexible I/O choices to fulfill vertical applications. The MIOe connector is ready for supporting additional extended interfaces and trend of future technologies which including DisplayPort, 4 PCIe x1, LPC, SMBus, USB2.0/USB3.0, Audio line out and Power.

The design of MI/O Extension took into account of soft-/hard-/firmware applications. These features are all parts of Advantech's thoughtful effort to

help integrators create their module designs most cost-effectively; in that, integrators can flexibly develop market-sensitive solutions and therefore get more promising business opportunities!

1.2 Features

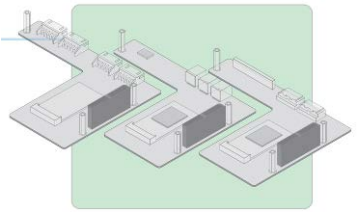
MIOe Unified Connector



MI/O extension has one unified MIOe connector which supports additional extended interfaces that gives more flexible support to bundled I/O modules, either from MI/O Extension solution provider or modules designed by the customer.
Through the interface, the functions can be:

- DisplayPort: HDMI, LVDS, DVI, CRT or eDP display type
- PCIe x 1: GbE, USB 3.0, SATA/RAID, FPGA or PCI expansion
- USB 2.0/ 3.0: Super speed storage, capture card, HD Webcam & display interface
- LPC: Legacy bus & Multi-UART, PS2, GPIO, FDD, IR, Parallel port from super I/O
- HD Audio: Line out, keep flexibility with selected amplifier
- SMBus: GPIO control, Smart battery/ Charger, W/R EEPROM
- Power: Supported by MI/O Extension SBC

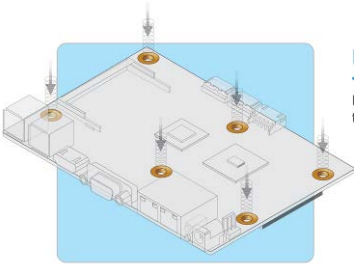
Expansion Module Options



Standard modules that ready for future interfaces and flexibility for varies vertical application demands.

- Display module or Communication module or Multiple I/O module from MI/O Extension solution vendors
- Customer's own MIOe module to secure domain knowhow

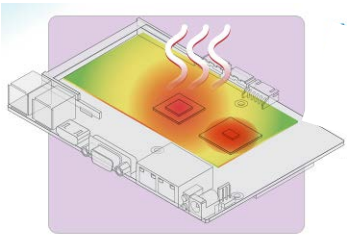
Unified System Screw Holes



MIOe Extension provide unified screw mounting holes for thermal solution assembly and system integration.

- Easy for system maintain
- Easy for platform upgrade

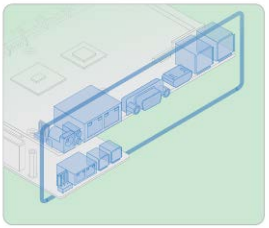
Concentrated Thermal Design



Traditional, the heat flow was designed on the topic and bottom sides of embedded boards. MI/O Extension SBC is designed with concentrated thermal design that all heat generation parts in top side, disperse the heat via the heat sink or the heat spreader with better result.

- Covers CPU, the Southbridge, Memory, Power and active IC
- Maximum thermal space
- Heat spreader/Heatsink Integration
- Simplify the system design
- Put thermal sensitive parts in bottom side to prevent thermal problems.

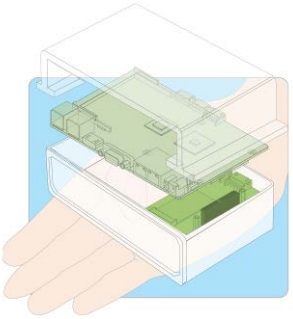
Reduced Cabling



MI/O Extension single board computers with unified I/O connector coastlines, and uniformly expanded compatibility of its CF card and mini PCIe locations. An area under the board is also designated for 2.5” hard disk. The structural uniformity helps eradicating possible problems with structural interference during future upgrades.

- Less cabling and Lockable connectors in bottom side.
- Reduce assembly schedule/ complex procedures and labor cost

Compact Mechanical Design



Compact and simple integration are the major concern of embedded system integrator.

- Reduce system assembly parts
- Saves up to 20% system space
- Optional heat spreader could have lowest total height

1.3 Name and Logo Usage

Manufacturers or distributors can use the MI/O Extension logo in promoting products if meet the Specification definition on the document.

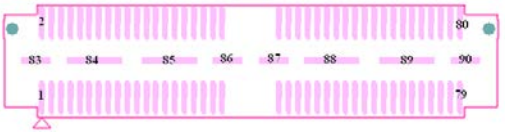
The name and logo of MI/O Extension and MIOe are trademarks of Advantech Technology in process of registration. These trademarks must be followed by the TM symbol.

1.4 Definitions

Signal Naming Convention	
REQ#	Active-low signals are indicated by a trailing '#' sign:
TX+, TX-	Differential pairs are indicated by trailing '+' and '-' signs:
A[0:31]	Bused signals are indicated by brackets, with LS bit first, MS bit last:
CBE[0:3]#	Bus brackets **may** appear anywhere in the signal name:
Pin and Signal Buffer Types	
Pin Types	
I	Input to the module
O	Output from the module
I/O	Bi-directional input / output signal
OD	Open drain output
Buffer Types	
CMOS	Logic input or output. Input thresholds and output levels **shall** be 80% of supply rail for high side and 20% of the relevant supply rail for low side.
PCIE	PCI Express compatible differential signal. Please refer to the PCI Express Specification for details. PCIE transmit pins (module outputs) **shall** be AC coupled on the module. PCIE receive pins (module inputs) **shall** be DC coupled on the COM ExpressTM module and **shall** be assumed to be AC coupled off-module, close to the signal source. If the target PCI Express device resides on the Carrier Board, the module PCIE receive lanes (target PCIE device transmit lanes) **shall** be AC coupled near the device on the Carrier Board. If the Carrier Board implements a PCIE slot, then these signals **shall** be AC coupled on the add-in card, not on the Carrier Board.
PCI	PCI 2.3 compatible signal. Please refer to the PCI Rev. 2.3 Specification for details.
SATA	SATA compatible differential signal. Please refer to the SATA Specification for details. All COM ExpressTM SATA signals shall be AC coupled on the module.
LVDS	Low Voltage Differential Signal – 330mV nominal; 450mV maximum differential signal.
USB	USB 2.0 compatible differential signal. Please refer to the USB 2.0 Specification for details.
REF	Reference voltage output. **May** be sourced from a module power plane.
Analog	Inputs and Outputs used for Audio are analog signals.
Power	Inputs used for power delivery to the module electronics.

Chapter 2 Pin Assignments

MI/O Extension has a number of connectors that allow you to configure your system to suit your application.



Pin	Name		Name	Pin
1	GND	Pin 83,84,85,86 GND	GND	2
3	PCIE_RX0+		PCIE_TX0+	4
5	PCIE_RX0-		PCIE_TX0-	6
7	GND		GND	8
9	PCIE_RX1+		PCIE_TX1+	10
11	PCIE_RX1-		PCIE_TX1-	12
13	GND		GND	14
15	PCIE_RX2+		PCIE_TX2+	16
17	PCIE_RX2-		PCIE_TX2-	18
19	GND		GND	20
21	PCIE_RX3+		PCIE_TX3+	22
23	PCIE_RX3-		PCIE_TX3-	24
25	GND		GND	26
27	PCIE_CLK+		LOUTL	28
29	PCIE_CLK-		LOUTR	30
31	GND		AGND	32
33	SMB_STB_CLK		NC	34
35	SMB_STB_DAT		NC	36
37	PCIE_WAKE#		NC	38
39	RESET#		NC	40
41	PowerOn	Pin 87,88,89,90 +5VSB	CLK33M	42
43	NC		LPC_AD0	44
45	DDP_HPD		LPC_AD1	46
47	GND		LPC_AD2	48
49	DDP_AUX+		LPC_AD3	50
51	DDP_AUX-		LPC_DRQ#0	52
53	GND		LPC_SERIRQ	54
55	DDP_D0+		LPC_FRAME#	56
57	DDP_D0-		GND	58
59	GND		USB0_D+	60
61	DDP_D1+		USB0_D-	62
63	DDP_D1-		GND	64
65	GND		USB1_D+/USB_SSTX+	66
67	DDP_D2+		USB1_D-/USB_SSTX-	68
69	DDP_D2-		GND	70
71	GND		USB2_D+/USB_SSRX+	72
73	DDP_D3+		USB2_D-/USB_SSRX-	74
75	DDP_D3-		GND	76
77	GND		USB_OC#	78
79	+12VSB		+12VSB	80

2.1 Audio

The CODEC of AC'97 Audio or HD Audio is established on the CPU board. The audio signal LOUTL, LOUTR and AGND are the interface for audio application.

2.1.1 Signal Descriptions

The following table shows audio interface signals, including pin number, signals, I/O and descriptions.

Pin No.	Audio	Pin Type	Power Rail	Description
28	LOUTL	O	1.2Vrms (Note2.1-1)	Analog output –Left channel.
30	LOUTR	O	1.2Vrms (Note2.1-1)	Analog output –Right channel.
32	AGND	AGND	0	Analog GND

Table 2.1-1 Audio Signal Description

Note 2.1-1 This value is just for reference, and the real one must refer to the corresponding codec spec.

2.1.2 Schematic Guidelines

The following schematics show audio amplifier application. For the CPU board, the codec with AC couple capacitor and EMI solution is present. On the I/O board, LDO is the better power solution for this application, and can supply clean power to audio amplifier. All the components should refer to analog ground AGND, and should reserve the resistor for current return path between AGND and GND.

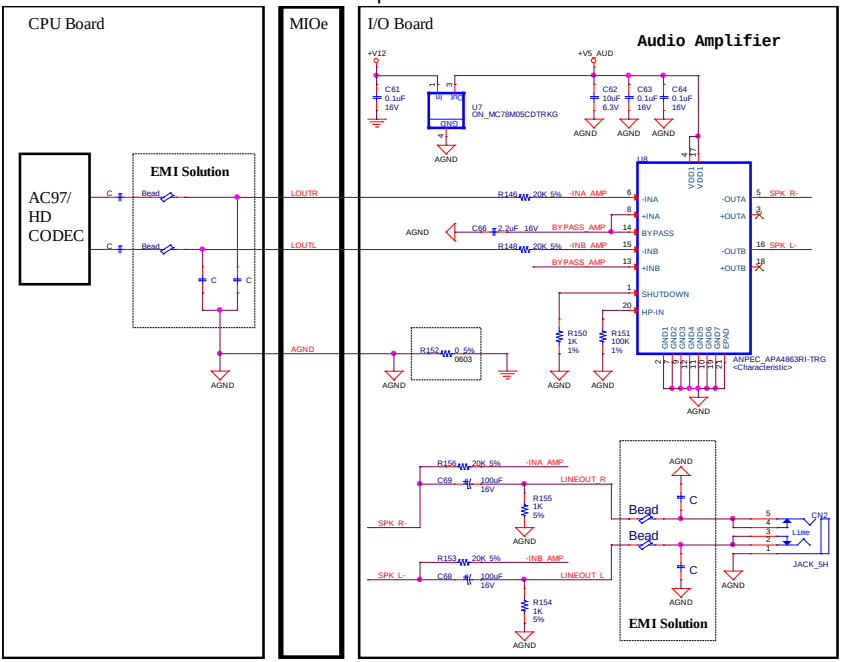


Figure 2.1-1 Audio Amplifier Application

2.2 DisplayPort

MIOe can support one DisplayPort for DP, HDMI or LVDS application. Some embedded applications, for example, LVDS should be working with video BIOS for setting panel information.

2.2.1 Signal Descriptions

The following table shows DisplayPort interface signals, including pin number, signals, I/O and descriptions.

Pin No.	Signal	Pin Type	Description
49	DDP_AUX+/ DDC_CLK	I/O DDP/ 3.3V I/O HDMI	DisplayPort AUX or DDC for HDMI interface
51	DDP_AUX-/ DDC_DAT	I/O DDP/ 3.3V I/O HDMI	
55	DDP_D0+	O DDP	DisplayPort Lane 0 or HDMI Data Lane
57	DDP_D0-	O DDP	
61	DDP_D1+	O DDP	DisplayPort Lane 1 or HDMI Data Lane
63	DDP_D1-	O DDP	
67	DDP_D2+	O DDP	DisplayPort Lane 2 or HDMI Data Lane
69	DDP_D2-	O DDP	
73	DDP_D3+	O DDP	DisplayPort Lane 3 or HDMI Data Lane
75	DDP_D3-	O DDP	
45	DDP_HPD	3.3V I CMOS	DisplayPort and HDMI hot-plug detection of active high

Table 2.2-1 DisplayPort

2.2.2 Schematic Guidelines for DP

For DP application, MIOe interface can provide four data lanes and one auxiliary pair without AC coupled capacitor and terminated resistors for DP devices or connector, and therefore I/O board must implement them close to devices or connector. DDP_HPD is an input pin of active high on MIOe interface, and its typical working voltage is 3.3 volt. It needs a level shift circuit that can shift the higher voltage down to 3.3 volt when the source signal is more than 3.3 volt.

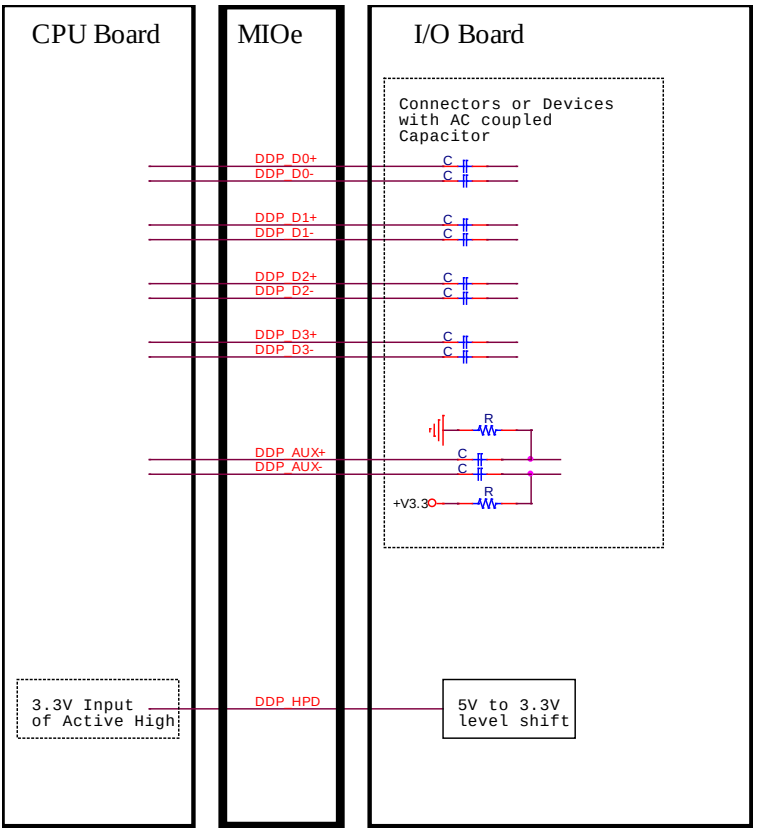


Figure 2.2-1 DP Application

2.2.3 Schematic Guidelines for HDMI

For HDMI application, MIOe interface can provide four data lanes without AC coupled capacitor and DDC interface for HDMI devices or connector, and therefore I/O board must implement them close to devices or connector. DDP_HPD is an input pin of active high on MIOe interface, and its typical working voltage is 3.3 volt. It needs a level shift circuit that can shift the higher voltage down to 3.3 volt when the source signal is more than 3.3 volt. DDC interface can be grouped into I/O pins of 3.3 volt, and it also needs level shift circuit when the source signals on I/O board are different from MIOe.

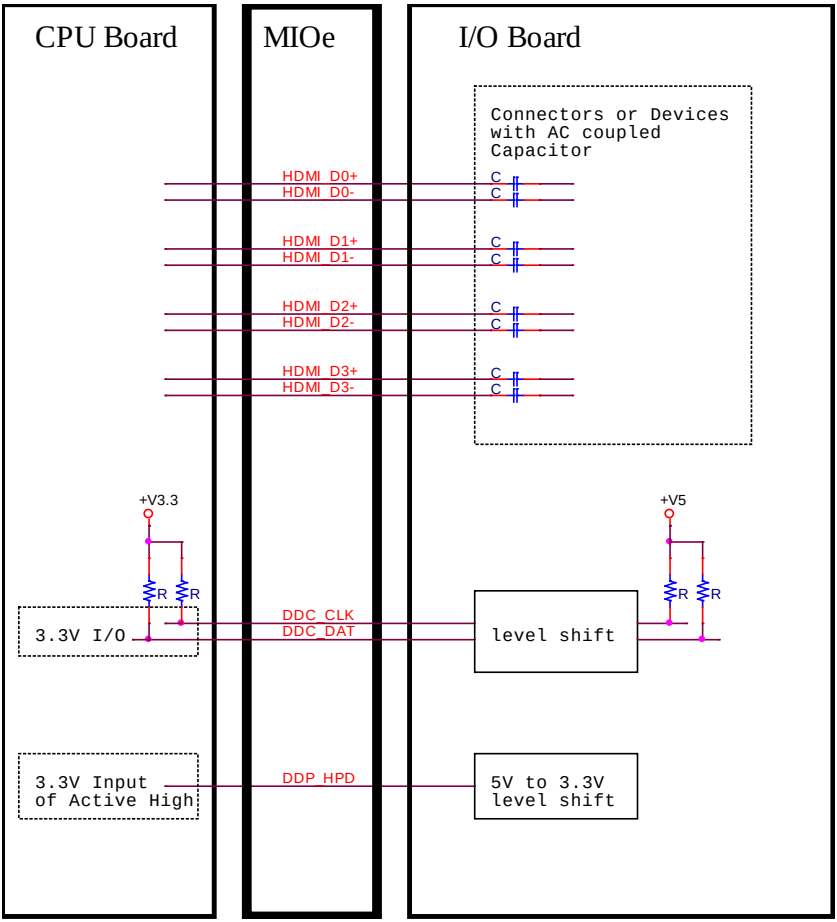


Figure 2.2-2 HDMI Application

2.3 LPC

MIOe provides a LPC interface to some devices as Super I/O, TPM, and others. For general application, Super I/O can accomplish some legacy functions, as Serial port, Parallel port, Floppy, IR, KBC and GPIO.

2.3.1 Signal Descriptions

Pin No.	LPC Interface	Pin Type	Description
42	LPC_CLK	O	LPC clock output - 33MHz
44	LPC_AD0	I/O	LPC multiplexed address, command and data bus
46	LPC_AD1		
48	LPC_AD2		
50	LPC_AD3		
52	LPC_DRQ#0	I	LPC serial DMA request
54	LPC_SERIRQ	I/O	LPC serial interrupt
56	LPC_FRAME#	O	LPC frame indicates the start of an LPC cycle

Table 2.3-1 LPC signal description

2.3.2 Schematic Guidelines

The I/O addresses for LPC devices on the CPU board are generally set as 2Eh and 29Ch. The recommendatory I/O address is 4Eh if there is LPC device on I/O board. The following figure shows the application.

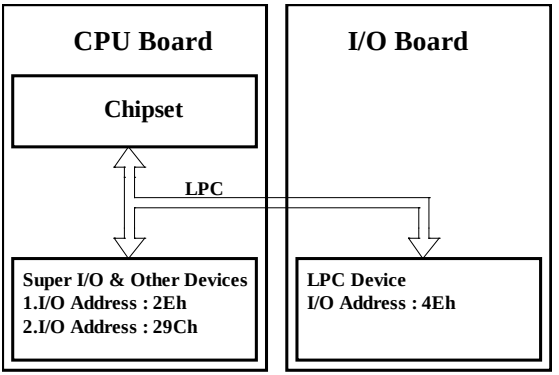


Figure 2.3-1 LPC Example

2.4 PCI Express

MIOe provides a PCI Express Bus interface that is compliant with the PCI Express Base Specification, Revision 1.0. It supports four general purpose PCI Express port (x1) and other configurations, for example, PCI Express port (x2) or PCI Express port (x4). PCI Express port (x1) is the default setting and other available configurations need to refer to product specification and request vendor's technical support.

2.4.1 Signal Descriptions

Pin No.	PCI Express Lanes (General Purpose)	Pin Type	Description
4	PCIE_TX0+	O PCIE	PCI Express Differential Transmit Pairs 0 through 3
6	PCIE_TX0-		
10	PCIE_TX1+		
12	PCIE_TX1-		
16	PCIE_TX2+		
18	PCIE_TX2-		
22	PCIE_TX3+		
24	PCIE_TX3-		
3	PCIE_RX0+	I PCIE	PCI Express Differential Receive Pairs 0 through 3
5	PCIE_RX0-		
9	PCIE_RX1+		
11	PCIE_RX1-		
15	PCIE_RX2+		
17	PCIE_RX2-		
21	PCIE_RX3+		
23	PCIE_RX3-		
27	PCIE_CLK+	O PCIE	Reference clock output for all PCI Express.
29	PCIE_CLK-		
37	PCIE_WAKE#	I CMOS	Power Management Event:Active low. Used to reactivate the PCI Express devices main power rails and reference clocks.

Table 2.4-1 PCI Express signals

2.4.2 Schematic Guidelines

Each PCI Express lane is AC coupled between its corresponding transmitter (TX) and receiver (RX). A 75-nF to 200-nF AC coupling capacitor is recommendable design. The following figure shows the interconnection between CPU and I/O boards. The AC coupling capacitors of TX+/- is present on CPU board. The AC coupling capacitors of RX+/- should be placed on the I/O board and closely to the transmitter pins of the PCI Express devices.
If some of the PCI Express port(s) is not implemented on MIOe, PCIE_TX[n]+/-, PCIE_RX[n]+/-, PCIE_CLK+/- and PCIE_WAKE# signals may be left unconnected, where 'n' is the port number.

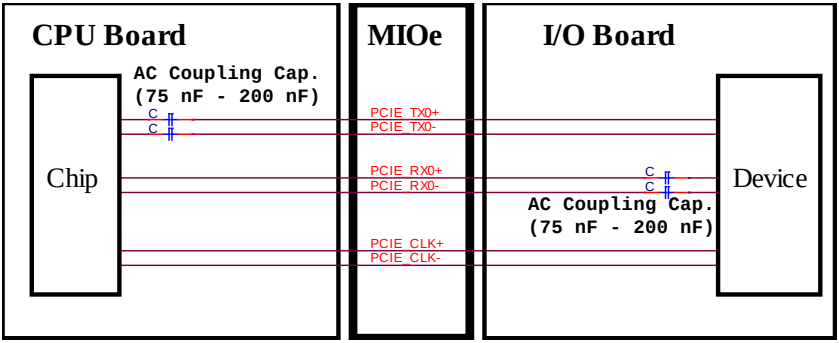


Figure 2.4-1 PCI Express Interconnection

MIOe only supports one differential clock for I/O board. I/O board needs added clock buffer if devices are more than one piece. The following figure shows this application.

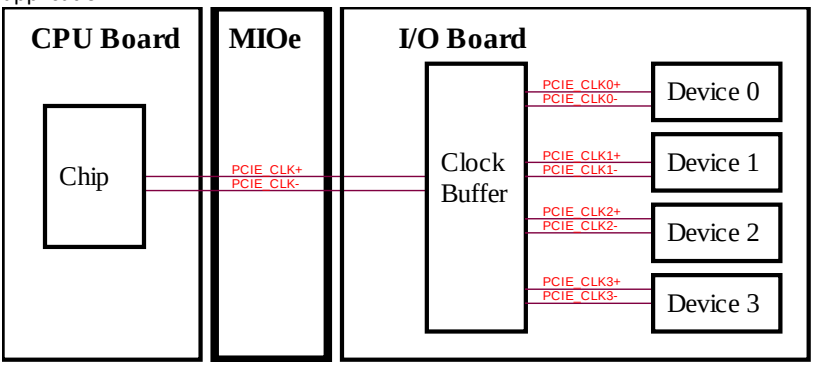


Figure 2.4-2 PCI Express clock buffer

2.5 SMBus

MIOe supports System Management Bus (SMBus) Specification, Version 2.0.

2.5.1 Signal Descriptions

Pin No.	Signal	Pin Type	Power Rail	Description
33	SMB_STB_CLK	I/OD	3.3VSB	System Management Bus bidirectional clock line.
35	SMB_STB_DAT	I/OD	3.3VSB	System Management Bus bidirectional data line.

Table 2.5-1 SMBus Signal Description

The following table is SMBus DC parameters for reference. Considering minimum VIL and maximum VIH, need to regard DC parameters of the SMBus controller on the CPU board. For general case, the minimum VIL of -0.5V and maximum VIH of 3.8V are reasonable value for reference when SMBus controller is supplied power with 3.3V. Other details need to refer to System Management Bus (SMBus) Specification Version 2.0.

Symbol	Min	Max	Units
VIL	-	0.8	V
VIH	2.1	-	V

Table 2.5-2 SMBus DC parameters

2.5.2 Schematic Guidelines

- The pull-up resistor size for the SMBus data and clock signals is dependent on the bus load (this includes all device leakage currents). Generally the SMBus device that can sink the least amount of current is the limiting agent on how small the resistor can be. The pull-up resistor cannot be made so large that the bus time constant (Resistance X Capacitance) does not meet the SMBus rise and time specification.

- The maximum bus capacitance that a physical segment can reach is 400 pF and the evaluation of capacitance is 3.3 pF per inch of trace length.

- The following figure is example circuit for SMBus. The SMBus controller on CPU board is powered by +V3.3SB power rail. SMB_STB_CLK and SMB_STB_DAT signals

are pulled high on CPU board, and don't need any pull-high resistor for SMBus on I/O board.

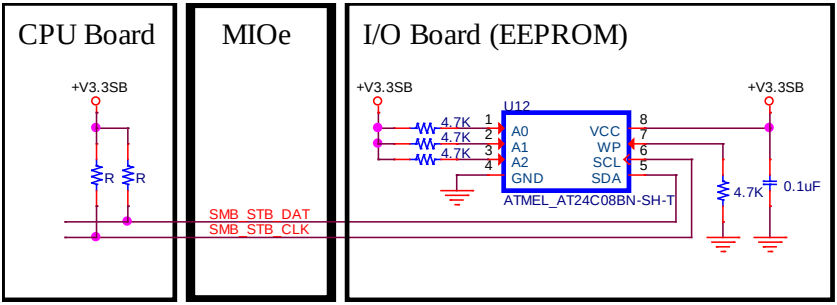


Figure 2.5-1 SMBus Example

Devices that are powered by the +V3.3SB well must not drive into other devices that are powered off. To avoid leakage current from +V3.3SB to +V3.3, this is accomplished with the bus switch. The figure below is the example for reference.

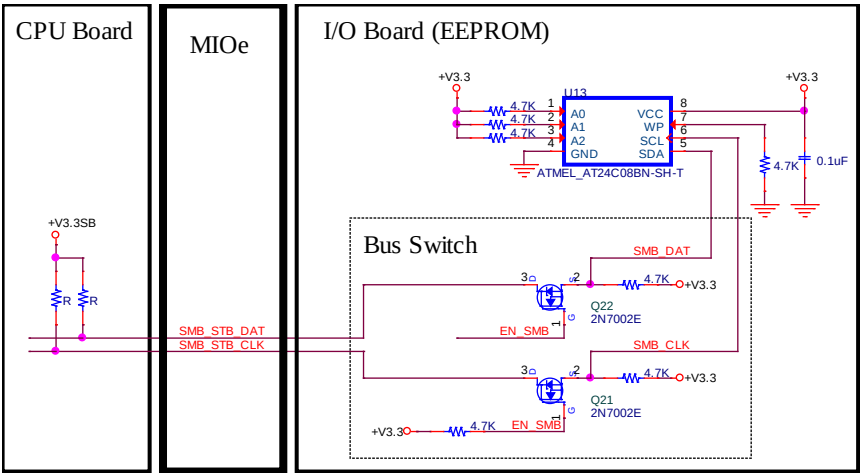


Figure 2.5-2 Bus Switch for SMBus

For multiple devices on SMBus, this is accomplished with the bus repeater to enhance driving capacity. PCA9515 is a recommendatory solution for this application.

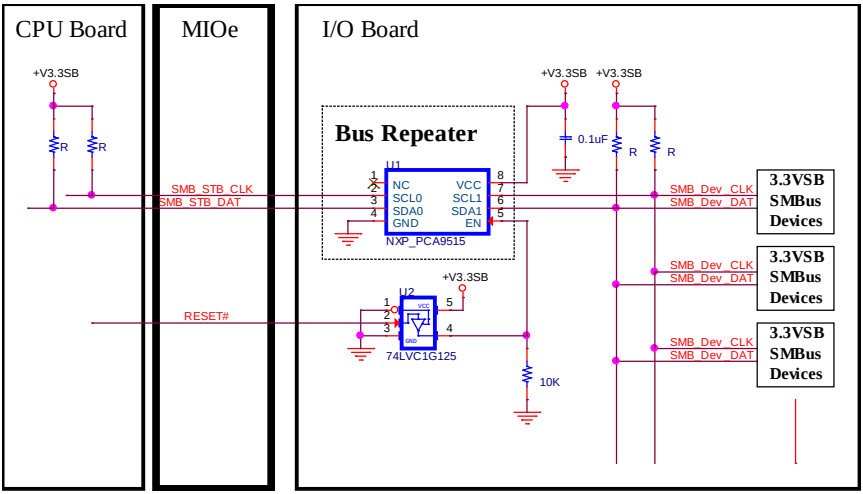


Figure 2.5-3 Bus Repeater for SMBus

2.6 USB

MIOe can provide up to three USB 2.0 ports, or one USB 2.0 port and one USB 3.0 port. For detailed configuration, please refer to product spec.

2.6.1 Signal Descriptions

Pin No.	Signal	Pin Type	Description
60	USB0_D+	USB 2.0	USB 2.0 differential pairs channel 0
62	USB0_D-	USB 2.0	
66	USB1_D+/ USB_SSTX+	USB 2.0/ USB 3.0	USB 2.0 differential pairs channel 1 or USB 3.0 differential pairs channel TX
68	USB1_D-/ USB_SSTX-	USB 2.0/ USB 3.0	
72	USB2_D+/ USB_SSRX+	USB 2.0/ USB 3.0	USB 2.0 differential pairs channel 2 or USB 3.0 differential pairs channel RX
74	USB2_D-/ USB_SSRX-	USB 2.0/ USB 3.0	
78	USB_OC#	I / 3.3VSB	USB over-current sense.

Table 2.6-1 USB Signal Description

2.6.2 Schematic Guidelines

USB_OC#, which is an input pin with pull-up resistor on CPU board, is used as over-current sense for USB port. Don't need to implement pull-up resistor on I/O board again. For two or more USB over-current detection, this pin can connect with two or more open drain buffers

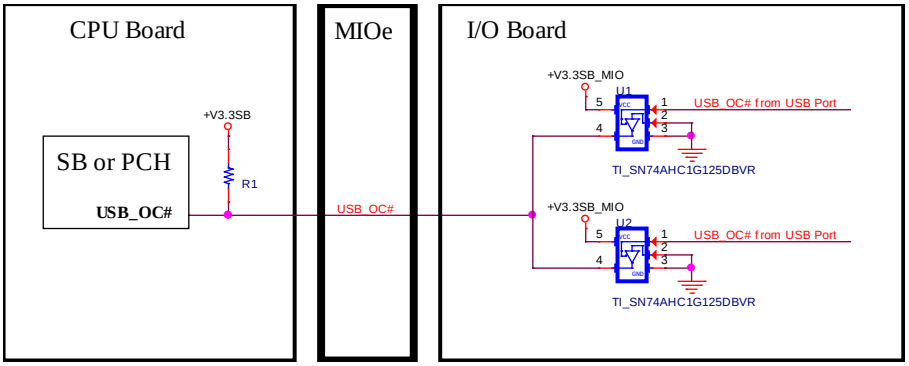


Figure 2.6-1 Demonstration for USB over-current detection

Considering EMI and ESD issue, the common mode choke and TVS (Transient Voltage Suppression) diode with low capacitance, which should be less than 1.0pF, are the recommendatory solution. For placement concern, EMI and ESD solution should be close to connector.

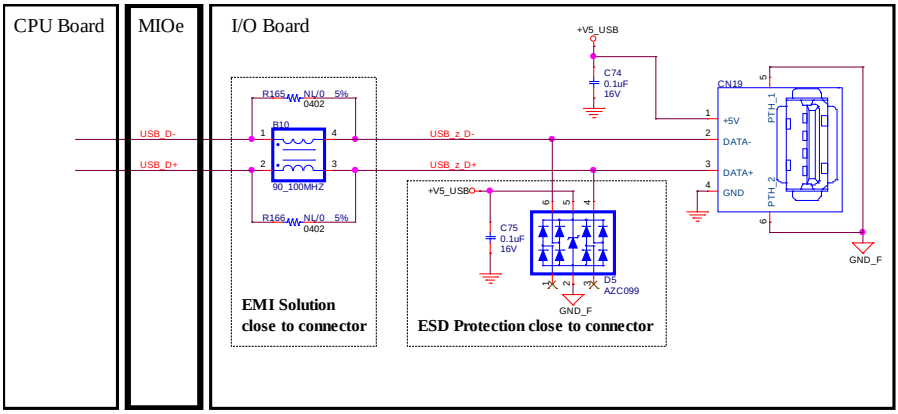


Figure 2.6-2 Demonstration for EMI and ESD design

Inspect USB 3.0 circuit, Serial AC coupling capacitors are must components on differential pair SSTX+/-. For differential pair SSTX+/-, Serial AC coupling capacitors which are present at I/O board can meet chipset design guideline, and must be close to EMI & ESD solution for external USB 3.0 connector. Figure 2.6-3 is the real demonstration, and other applications need to refer to relevant documents.

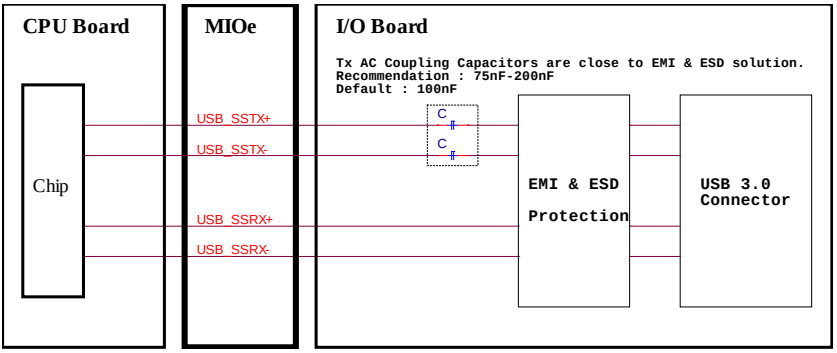


Figure 2.6-3 Demonstration for USB 3.0 AC coupling capacitor

2.6.3 Layout Guidelines

See Section 2.7 General Layout Guideline for reference.

2.7 General Layout Guidelines

This section provides general layout guideline for high speed signals, PCI Express, USB and DisplayPort.

2.7.1 Impedance

In a high-speed signaling environment, signal trace impedances must be controlled in order to maintain good signal quality across the motherboard. Signal trace impedance is a function of the following three factors:

• Motherboard stack up
• Dielectric constant of the PCB substrate
• Signal trace width and thickness

2.7.2 Crosstalk

The following list of recommendations should be followed to help reduce the crosstalk on the motherboard:

- Do not allow high-speed signals to cross plane splits.
- Reference critical signals to ground planes.
- Do not cut ground planes unless it is absolutely necessary.
- Reduce the length of signals that are routed parallel.
- Provide analog signals with guard shields or guard rings.
- Keep analog signals away from digital signals.

2.7.3 Reference Planes

The high-frequency return path for any signal lies directly beneath the signal on the adjacent layer. Providing a solid plane underneath a signal greatly reduces problems with signal integrity, timing, and EMI because the plane provides a direct return path for that signal. There are two cases where a signal can change its reference plane: crossing a plane split or changing signal layers. If either of these are unavoidable, techniques must be used to minimize the negative impact caused by changing reference planes.

2.7.4 Crossing Plane Splits

When crossing a plane split, a 0.1-μF or 0.01-μF stitching capacitor with a 0402 or smaller body size should be used. Place the stitching capacitors as close as possible to the traces crossing the split, as shown in Figure 2.7-1.

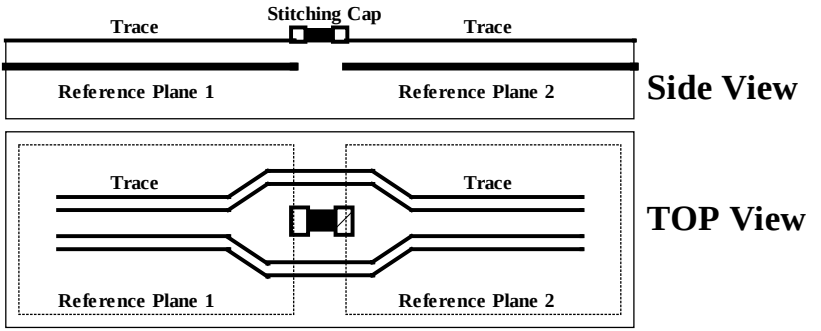


Figure 2.7-1 Trace Crossing Plane Splits

2.7.5 Referencing Different Plane Layers

When signal traces change layers, ground stitching via should be placed amongst the signal via in order to provide a return path. Place the stitching via as close as possible to the signal via, as shown in Figure 2.7-2.

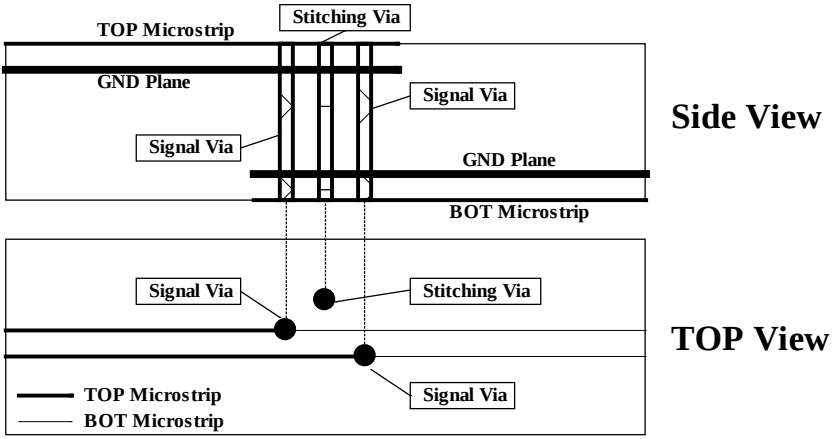
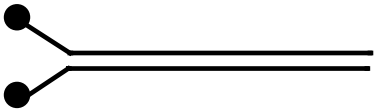


Figure 2.7-2 Ground Stitching Via

2.7.6 Differential pair routing

It is important to maintain routing symmetry between the two signals of a differential pair. Failure to maintain symmetry between the signals of the differential pair will introduce an AC common mode voltage.

Preferred: Symmetrical Routing



Avoid: Non-symmetrical Routing

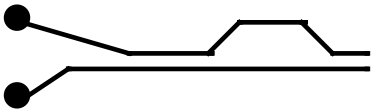


Figure 2.7-3 Symmetrical Routing for differential pair

There is only one lane, and each link will be routed to different devices at varied locations of the board, it is most practical to route the TX signal and the RX signal of that lane next to each other on the same layer.

Differential-Pair length matching should be maintained segment-to-segment. Examples of segments might include breakout areas, route to connect vias, route to connect a connector, and so forth.

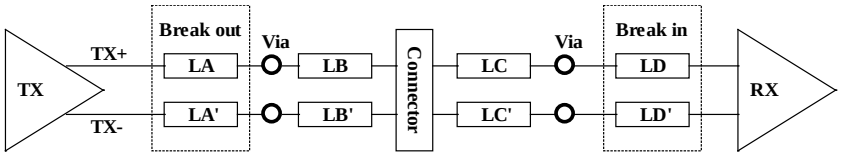


Figure 2.7-4 length matching example

When trace length matching compensation occurs, it should be made as close as possible to the point where the variation occurs, as shown in Figure 2.7-5.

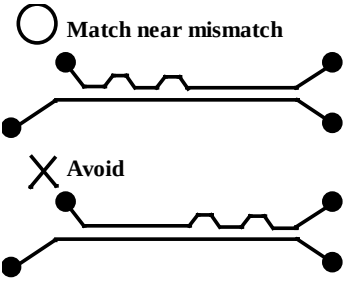


Figure 2.7-5 length matching compensation near mismatch

When serpentining is needed to match lengths, the following guidelines should be maintained. The trace spacing should not become greater than 2 times the original spacing. The length of the increased spacing should not be greater than 3 times the trace width.

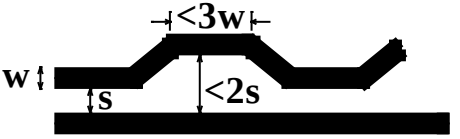


Figure 2.7-6 serpentine rule

Chapter 3 Power Management & Power Delivery

This chapter provides the power supply design recommendations for customer's reference.

3.1 Signal Descriptions and MIOe Power Rating

The following table shows the power management signal, including pin number, signal naming, pin type, power rail, and description. The following section will introduce the real application for reference.

Pin No.	Signal	Pin Type	Power Rail	Description
39	RESET#	O	3.3V	CPU board asserts RESET# to reset devices on the I/O board (e.g., LPC devices, PCIe devices, LAN, etc.).
41	PowerOn	O	3.3V	PowerOn can be used with application that needs to turn on the power for MIOe board.

Table 3.1-1 Power Management Signal

The following table shows independently the power rating for MI/O- Compact and MI/O-Ultra CPU board. Figure 3.1-1 can explain the overall power flowchart in the system and define the symbol "I5Vmio", "I5Vsys" and "I5Vall".

Pin No.	Signal	Pin Type	Power Rail	Current Symbol	MIO-5xxx Current Rating	MIO-2xxx Current Rating
79,80	+V12SB	Power	12VSB	I12Vmio	2000 (mA)	2000 (mA)
87,88,89,90	+V5SB	Power	5VSB	I5Vmio	3000 (mA)	2000 (mA)

Table 3.1-2 MIOe Board Power Rating

The following figure is a system power flowchart. *I12Vmio* and *I5Vmio* are the current rating for I/O board, *I5Vsys* is the current rating for system I/O devices and *I5Vall* is the current rating of +12VSB to +5VSB power module. The following equation is a necessary result.

I5Vall =I5Vmio+ I5Vsys

The power rail 5VSB and 5V are isolated by MOSFET, but they have the same power source. To evaluate 5V power budget, must be concerned both 5VSB and 5V system I/O devices, for example SATA HDD, CF card, PS2 keyboard and mouse. The following equation indicates the truth of power flow.

I5Vsys = Ia + Ib + Ic + Id + Ie

where

Ia: SATA HDD power consumption current from power rail +V5
Ib: CF or CFast power consumption current from power rail +V5
Ic: LCD Panel power consumption current from power rail +V5
Id: PS2 KB/MS power consumption current from power rail +V5SB
Ie: USB device power consumption current from power rail +V5SB

MIOe board can use more power from CPU board if the customer can reduce the power consumption from system I/O devices. But the equation (I5Vall = I5Vsys + I5Vmio) must be obeyed. In other words, CPU board can use all the power from power module if without MIOe board.

Current	Description	MIO-5xxx Current Rating	MIO-2xxx Current Rating
I5Vsys	It is current rating for 5V and 5VSB system I/O devices connected with CPU board.	2000 (mA)	1000 (mA)
I5Vall	It is the current rating of +12VSB to +5VSB power module on CPU board.	5000 (mA)	3000 (mA)

Table 3.1-3 CPU Board Power Rating

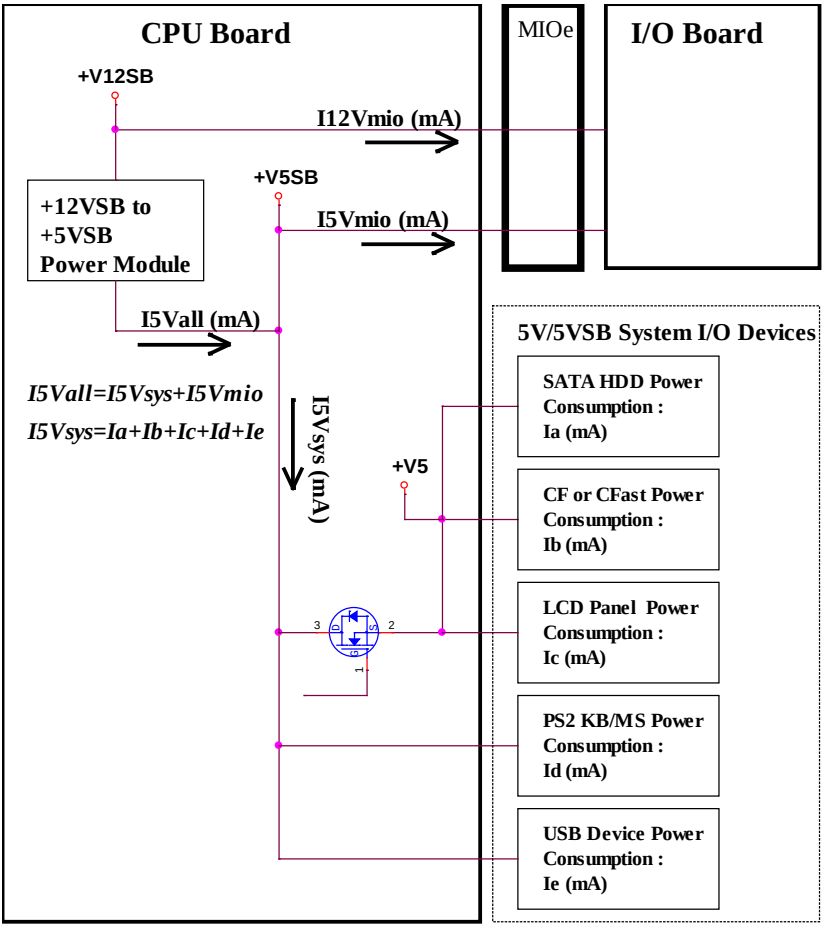


Figure 3.1-1 System Power Flowchart with MIOe board

3.2 CPU Board Power rating without MIOe Board

The CPU board can be used alone without MIOe board. It is easy to evaluate power budget of 5V power rail. All the current rating of +12VSB to +5VSB power module can be used with 5V and 5VSB system I/O devices connected with CPU board, for example SATA HDD, CF, LCD panel, PS2 and USB.

The following figure shows overall system power flowchart and the following table shows the current rating for MI/O-Compact and MI/O-Ultra CPU board without MIOe board. On the figure, *I5Vsys* is the current rating for system I/O devices and *I5Vall* is the current rating of +12VSB to +5VSB power module. The following equation is a necessary result.

I5Vall =I5Vsys

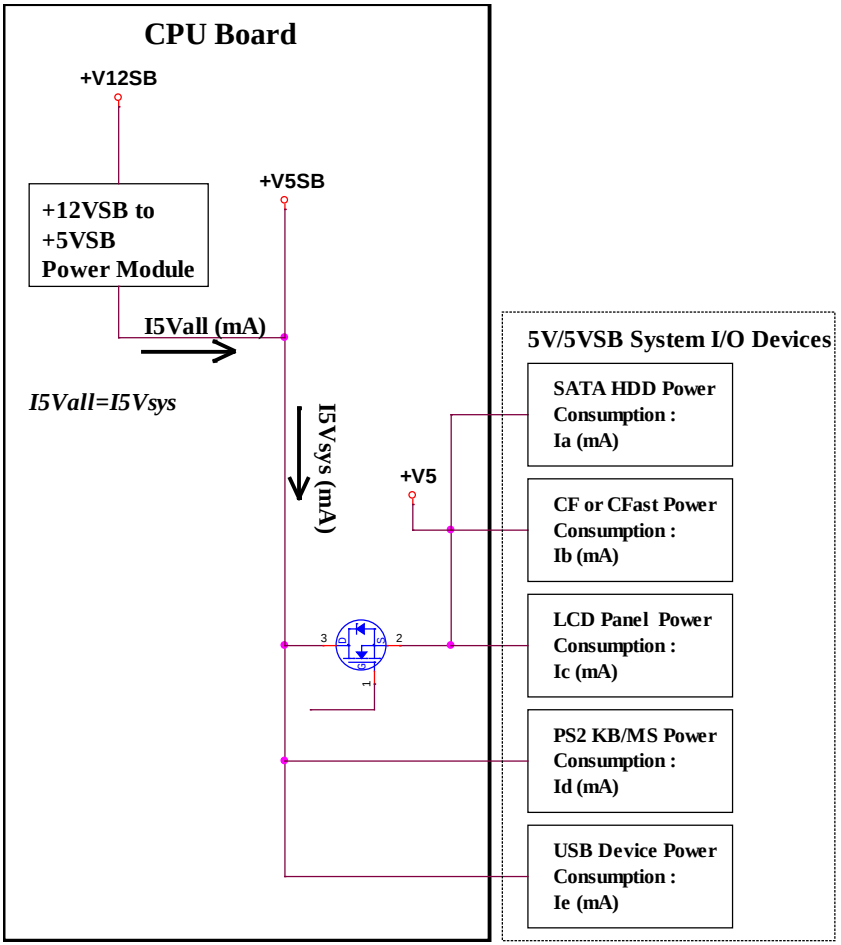


Figure 3.2-1 System Power Flowchart without MIOe board

Current	Description	MI/O Extension Compact Series Current Rating	MI/O Extension Ultra Series Current Rating
I5Vsys	It is current rating for 5V and 5VSB system I/O devices connected with CPU board.	5000 (mA)	3000 (mA)
I5Vall	It is the current rating of +12VSB to +5VSB power module on CPU board.	5000 (mA)	3000 (mA)

Table 3.2-3 CPU Board Power Rating without MIOe Board

3.3 DC Specifications

Pin No.	Signal	Pin Type	Power Rail	Voltage Typical	Voltage Min.	Voltage Max.
79,80	+V12SB	Power	12VSB	12V	10.8V	13.2V
87,88,89,90	+V5SB	Power	5VSB	5V	4.75V	5.25V

Table 3.3-1 MIOe DC specification

3.4 CPU board Supply Power to MIOe Board

The following figure is the application that CPU board can fully supply power to I/O board. In lower power consumption case, CPU board can provide enough power to meet I/O board requirement and PowerOn is the must control signal to turn on the main power +V12, +V5 and +V3.3.

In this case, the power +V12, +V5 and +V3.3 are obtained from MOSFET (Q1, Q3 and Q4) whose gate is controlled by signal PowerOn. The rising timing can be fine tuned by the soft start circuit (R2, R4 and C1 for Q1, R7, C2 and C3 for Q3/Q4) connected with the individual MOSFET. MOSFET with soft start circuit can reduce inrush current

when it is turned on. But rising timing requirement must be concerned, the following power-on sequence and timing parameters are necessary conditions.

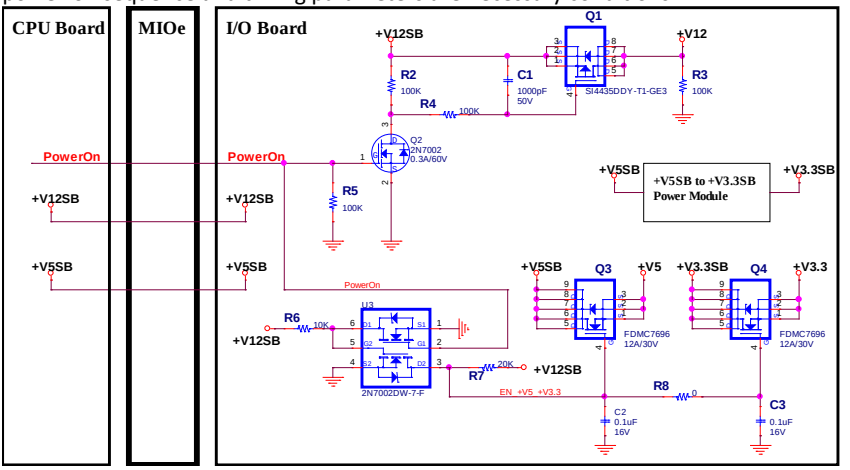


Figure 3.4-1 CPU board supply power to I/O board

The following figure is power sequence requirement for I/O board. CPU board can't work normally, if I/O board doesn't follow up this specification.

I/O Board Power-On Sequence

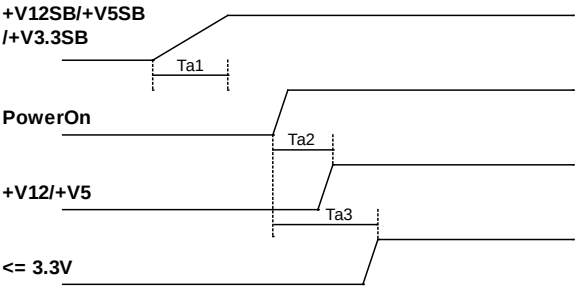


Figure 3.4-2 I/O board power-on sequence

	Min. (ms)	Max. (ms)	Description
Ta1	0	40	+V12SB/+V5SB/+V3.3SB active to +V12SB/+V5SB/+V3.3SB ready
Ta2	0	20	PowerOn active to +V12/+V5 ready
Ta3	0	20	PowerOn active to other power rail ready

Table 3.4-1 Timing parameters

3.5 External Power Source for CPU and MIOe Board

For some application, CPU board can't supply enough power to I/O board. It is a recommendable solution to plug in external power supply for CPU and I/O board. The following figure shows the simple circuits and power-on sequence for this application. Some check points are very important as the below and designer must follow up these suggestions.

1. The single power supply must provide power for CPU and I/O board simultaneously.
2. On the I/O board, the power pin (+V5SB & +V12SB) of MIOe connector must be left open.
3. On the I/O board, the GND pin of MIOe connector must be connected.
4. Use PowerOn as control signal to turn on main power +V12_MIOe and +V5_MIOe and meet the power-on sequence and timing parameters as the figure and table below.

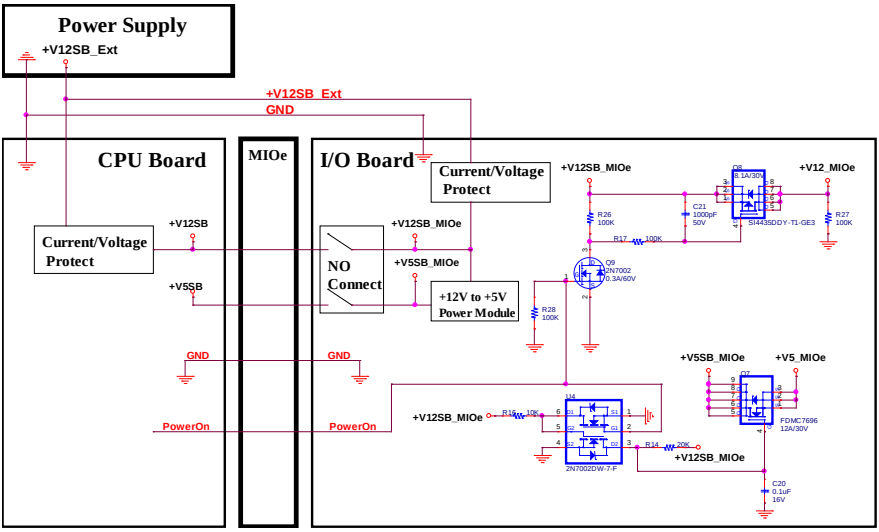


Figure 3.5-1 External power source for CPU and I/O board

I/O Board Power-On Sequence

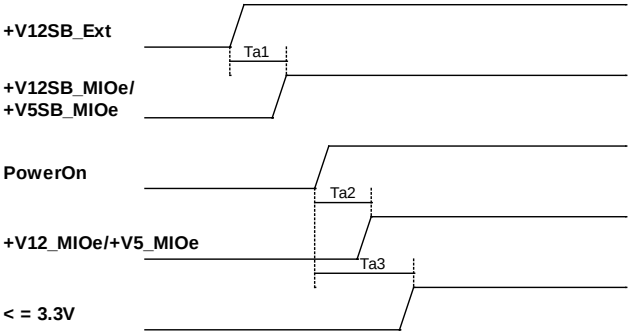


Figure 3.5-2 I/O board power-on sequence

	Min. (ms)	Max. (ms)	Description
Ta1	0	40	+V12SB_Ext active to +V12SB_MIOe/ +V5SB_MIOe/+V3.3SB_MIOe ready
Ta2	0	20	PowerOn active to +V12_MIOe/+V5_MIOe ready
Ta3	0	20	PowerOn active to other power rail ready

Table 3.5-1 Timing parameters

3.6 Other Design Concern

PowerOn is the control signal to turn on main power rail and its maximum high-level and low-level output current is limited to under 1mA for I/O board. For high driving current application, 74AHCT1G125 is the recommendatory solution for buffer. The following figure shows this application and the following table is operating condition of IC.

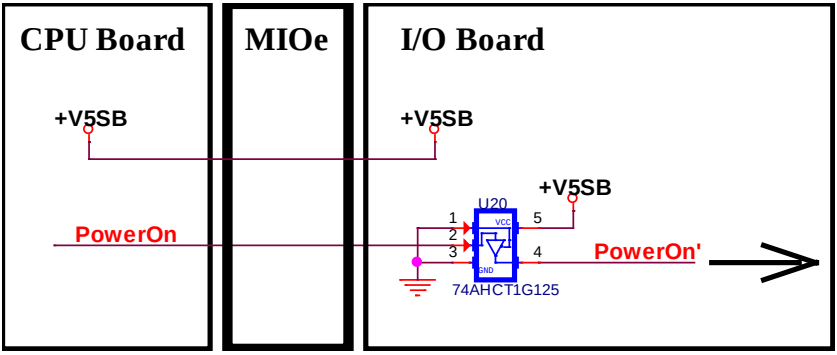


Figure 3.6-1 PowerOn buffer

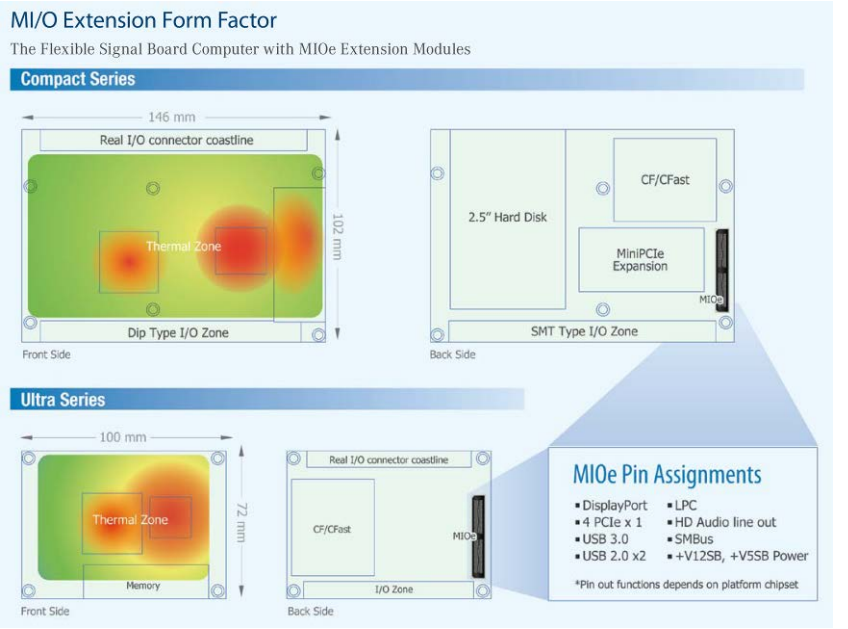
		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	5.5	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		–8	mA
I_{OL}	Low-level output current		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20	ns/V
T_A	Operating free-air temperature	–40	85	°C

Table 3.6-1 74AHCT1G125 operating condition

RESET# is reset signal and its maximum high-level and low-level output current is limited to under 1mA for I/O board. For high driving current application, 74AHCT1G125 is the recommendatory solution for buffer.

Chapter 4 Mechanical Characteristics

4.1 Mechanical Design



4.1.1 Mechanical Drawing

MI/O Extension SBC with 2 series, one is MI/O-Compact and another one is MI/O-Ultra SBC.

The PCB size of the MI/O-Compact is 203mm x 146mm, and 100 x 72mm for MIO-Ultra.

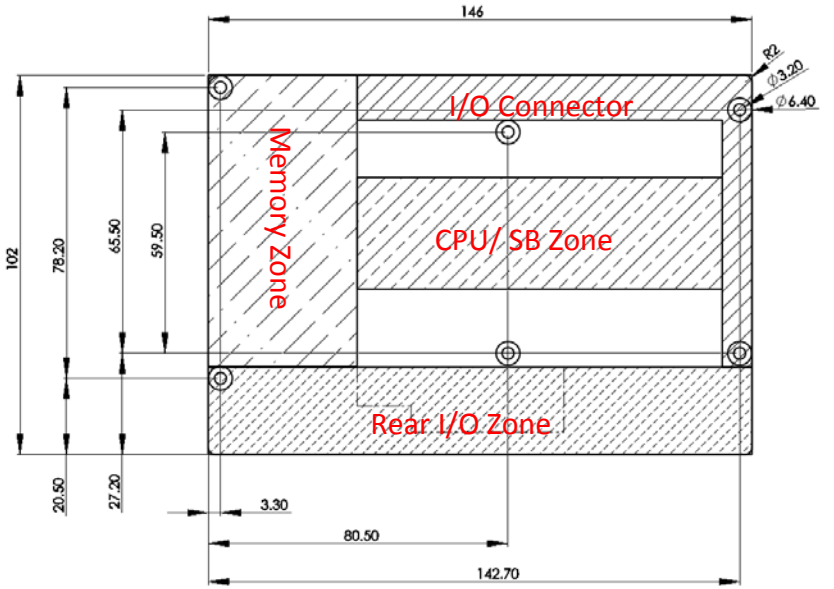
The PCB thickness is designed at 1.6mm(+/- 10%).

The mounting holes shown in below are intended for mounting the MI/O Extension SBC, MIOe module and thermal solution combination.

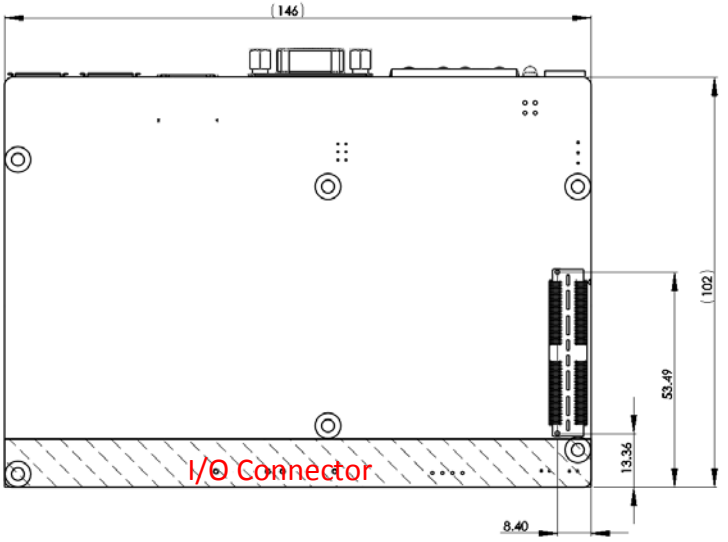
The unit shown on below drawing is in millimeters.

4.1.2 MI/O-Compact Drawing

MI/O-Compact Top side: (mm)



MI/O-Compact Bottom side: (mm)



The component maximum height in bottom side is 11mm on MI/O-Compact SBC.

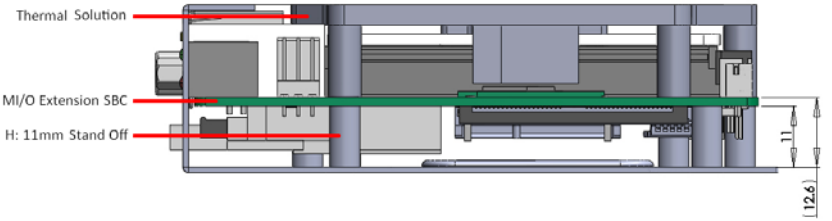
Tolerances shall be ± 0.25mm [±0.010”], unless noted otherwise.
The tolerances on MIOe connector locating peg holes (dimensions [8.40, 13.36] shall be ± 0.10mm [±0.004”].

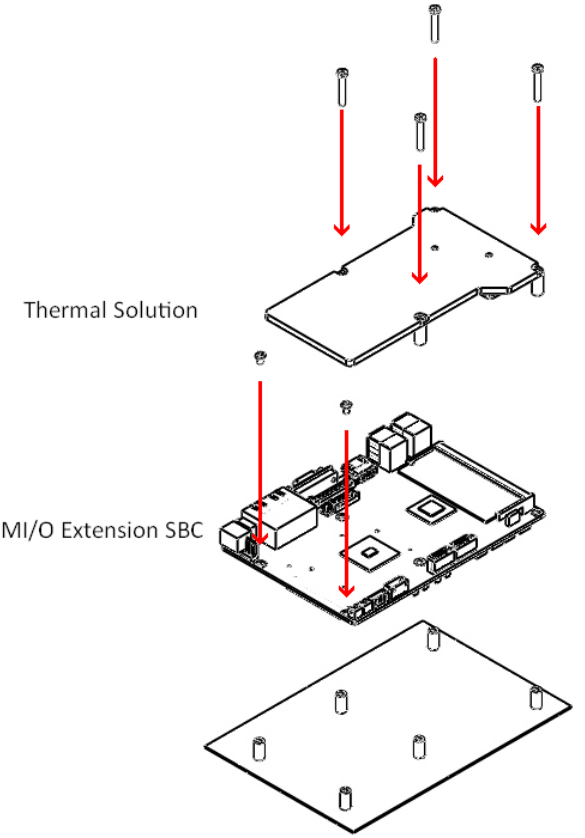
The 6 mounting holes shown shall use 6.4mm diameter pads and shall have 3.2mm plated holes, for use with M3 hardware. The pads shall be tied to the PCB ground plane.

Stand off: M3x D5.5x L11mm

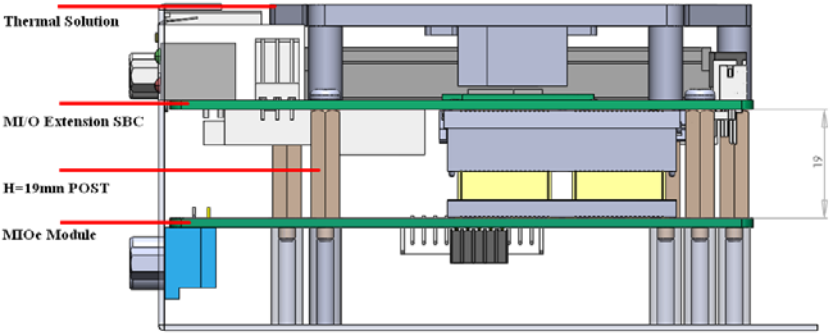
MI/O-Compact Installation: (mm)

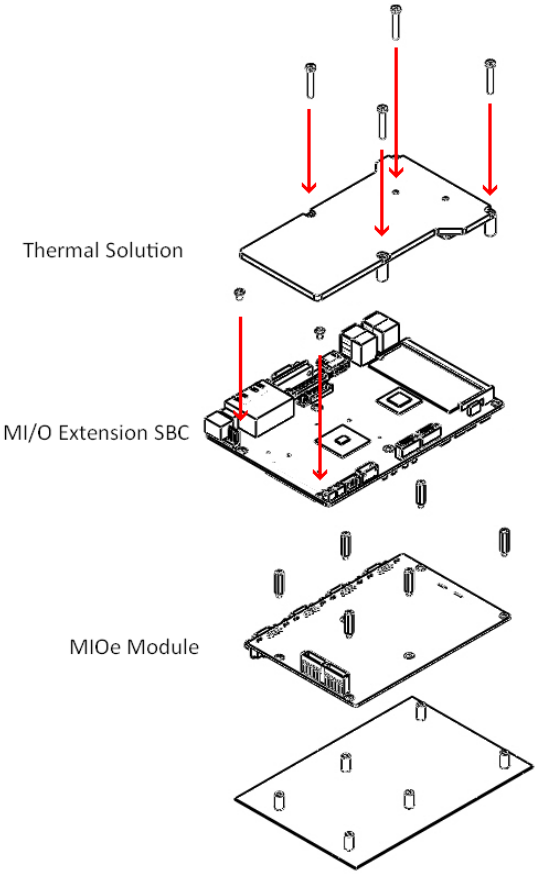
- Without MIOe module installation:





- With MIOe module installation:

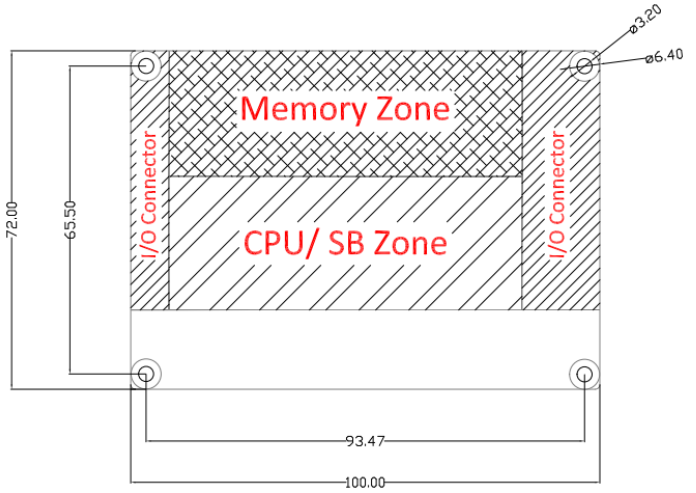




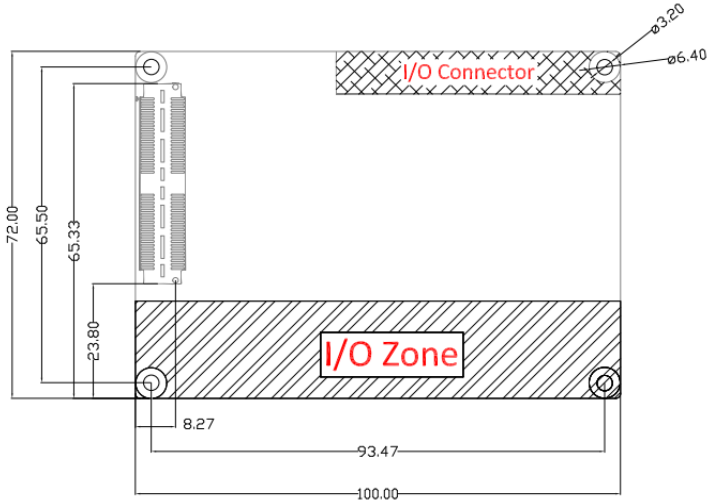
The component maximum height in top side of MIOe module is 7mm.

4.1.3 MI/O-Ultra Drawing

MI/O-Ultra Top side: (mm)



MI/O-Ultra Bottom side: (mm)



The component maximum height in bottom side is 15mm on MI/O-Ultra SBC.

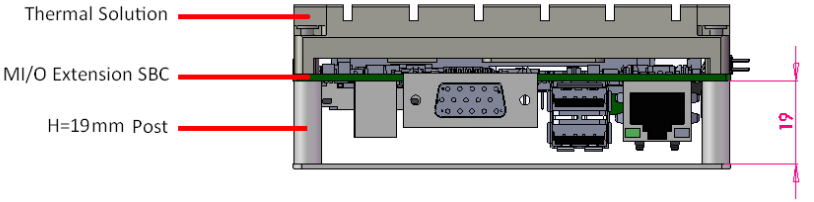
Tolerances shall be ± 0.25mm [±0.010”], unless noted otherwise.
The tolerances on MIOe connector locating peg holes (dimensions [8.27, 23.80] shall be ± 0.10mm [±0.004”].

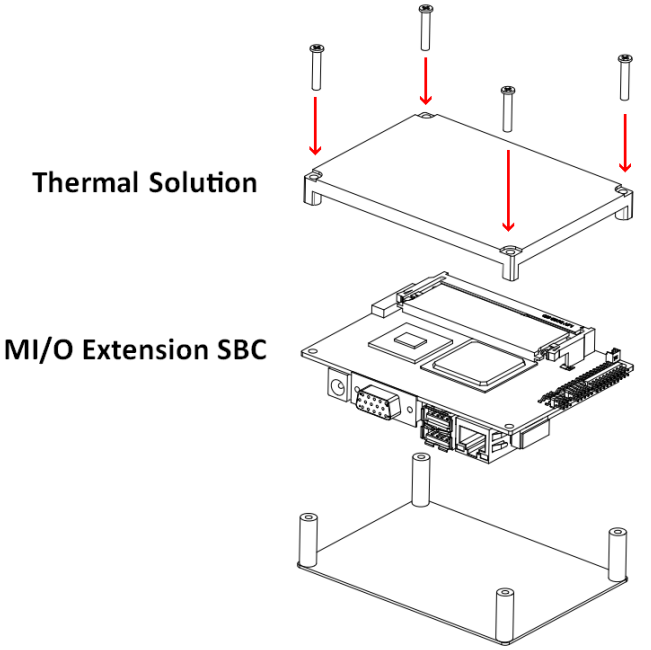
The 4 mounting holes shown shall use 6.4mm diameter pads and shall have3.2mm plated holes, for use with M3 hardware. The pads shall be tied to the PCB ground plane.

Stand off: M3x D5.5x L11mm

MI/O-Ultra SBC Installation: (mm)

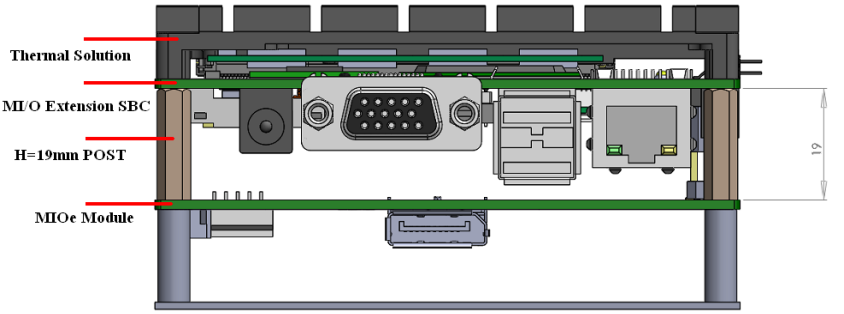
- Without MIOe module installation:

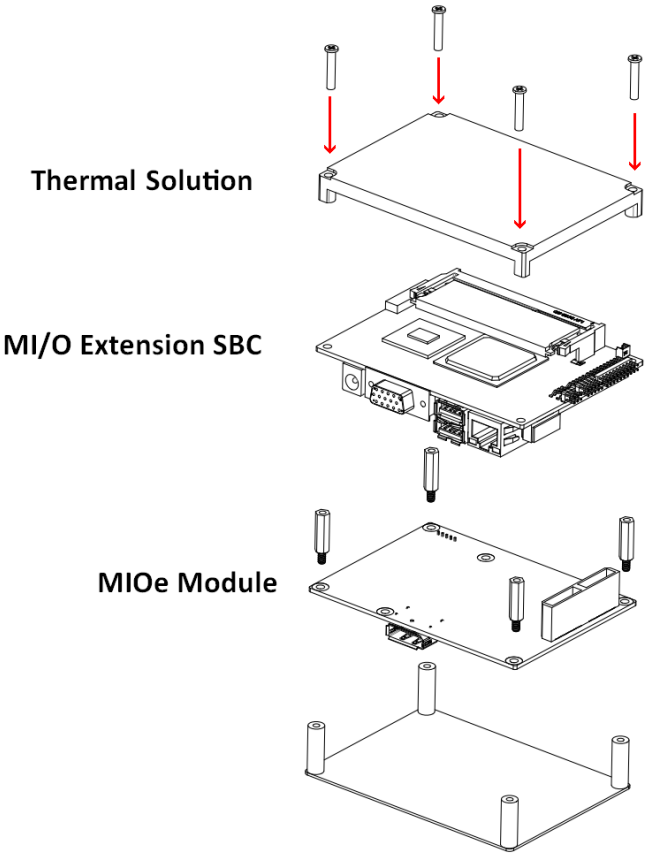




The component maximum height in top side of MIOe module is 7mm.

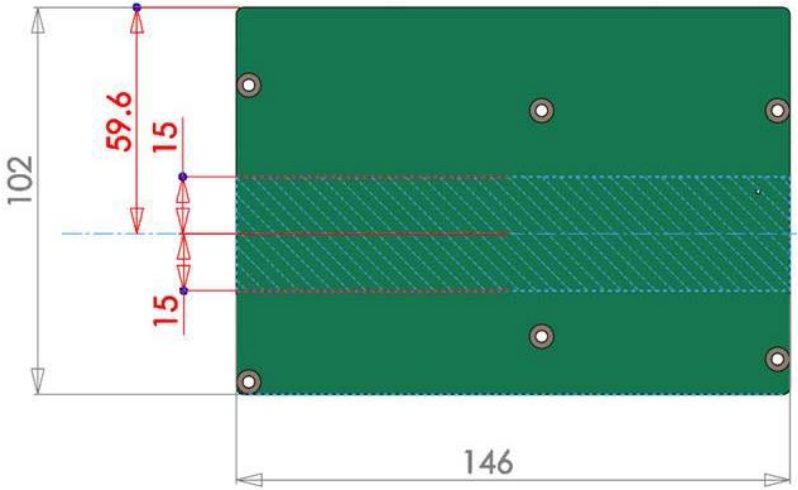
- With MIOe module installation:



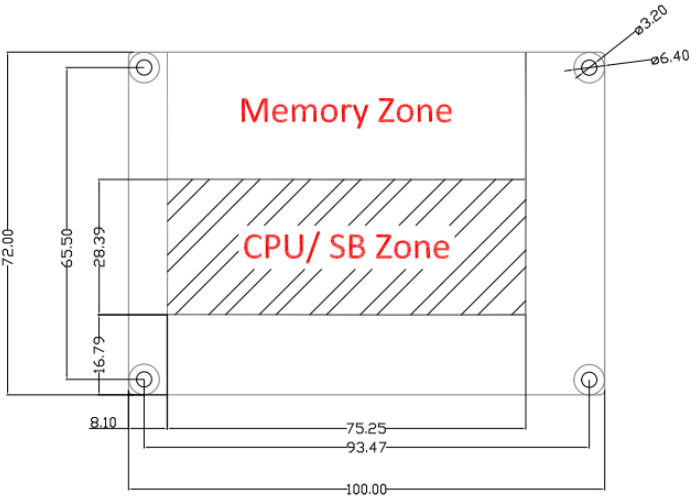


4.1.4 Thermal Design

MI/O-Compact : Thermal generation parts in the gray zone.



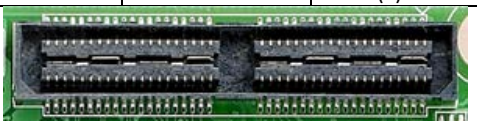
MI/O-Ultra SBC: Thermal generation parts in the gray zone.



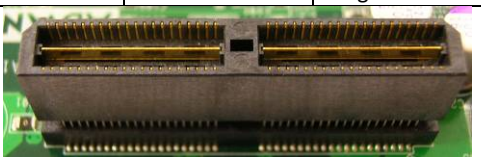
4.1.5 MIOe Connector

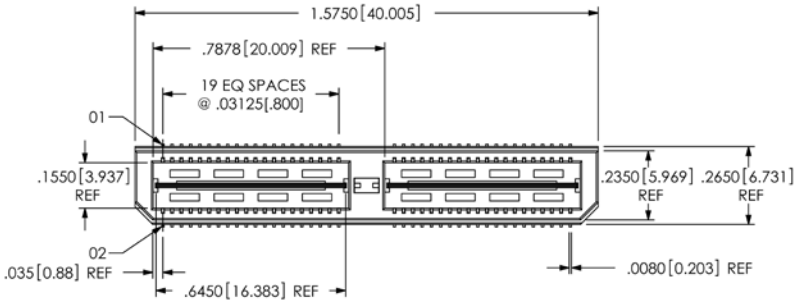
The connector vendor is Samtec.

Connector location	Samtec P/N	Description
Connector on CPU Board	QSE-040-01-L-D	B/B Conn. 40x2P 0.8mm 180D(F) SMD

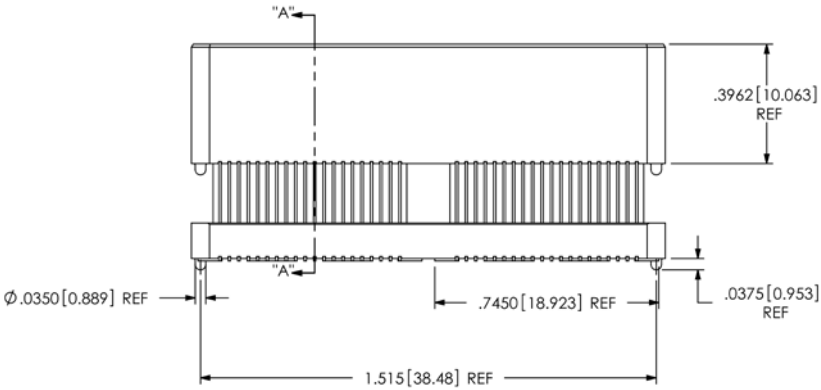


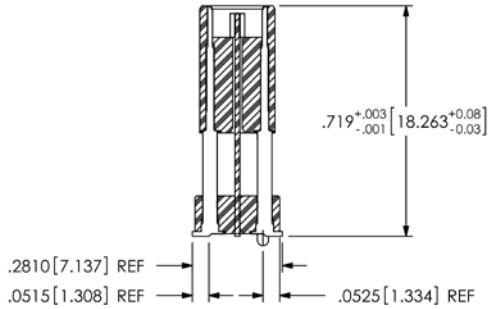
Connector location	Samtec P/N	Description
Connector on MIOe module	REF-165028-01	B/B Conn. 40x2P 0.8mm 180D(M) SMD, 19mm mating height





Samtec Website: http://www.samtec.com/





SECTION "A"-"A"
SCALE 2 : 1