Ruggedized Architecture Hardware Specification

Version 2.0 Dec, 2015

REVISION HISTORY

Rev	Date	Notes
0.1	June 18, 2014	Initial version
0.2	Nov 11, 2015	First version
0.3	Dec 01, 2015	Update description for pin defines
2.0	Dec 17, 2015	Release version

RTX

Contents

1. Introduction

1.1 General Introduction

The RTX 2.0 (Ruggedized Technology eXtended) specification is a Ruggedized Standard platform designed for demanding applications. Through its innovative mechanical and electrical design, products designed with RTX2.0 can perform in complex and challenging environments such as military , logistics, transportation / fleet management, and many other industrial applications.

RTX 2.0-based module includes four board-to-board connectors for all I/O signals and mounting hole locations. The asymmetrical mounting hole design provides two advantages. Firstly, they provide an effective mistake-proof solution during assembly. Secondly, the defined mounting holes not only allow screw fixing onto the carrier board via metal nuts, but also provide superior heat dispersion. As for I/O expansion, RTX 2.0 uses the standard 400-pin definition through four connectors providing customers with high I/O expandability. Also, it takes the latest interface trends into account. RTX 2.0 supports both USB 3.0 and MIPI/CSI-2 (Camera interface) to offer better expansion that can meet a variety of different requirements.

Applications included:

- Military
- Industrial control system
- Transportation/Fleet management
- Robotic
- Power Equipment
- Inspection Equipment

1.2 Purpose of this document

This document defines the Module mechanical, electrical, signal and thermal parameters at a level of detail sufficient to provide a framework for RTX Module and Carrier Board.

1.3 Document and standard reference

- ***CAN ("Controleer Area Network") Bus Standards – ISO 11898, ISO 11992 , SAE J2411***
- ***CSI-2 (Camera Serial Interface version 2)*** The CSI-2 standard is owned and maintained by the MIPI Alliance ("Mobile Industry Processor Alliance") (http://www.mipi.org)
- ***DisplayPort*** and ***Embedded DisplayPort*** These standards are owned and maintained by VESA ("Video Electronics Standards Association") (**www.vesa.org**)
- ***D-PHY*** CSI-2 physical layer standard – owned and maintained by the MIPI Alliance (**www.mipi.org**)
- ***DSI (Display Serial Interface)*** The DSI standard is owned and maintained by the MIPI Alliance ("Mobile Industry Processor Alliance") (**www.mipi.org**)
- ***eMMC ("Embedded Multi-Media Card")*** The eMMC electrical standard is defined by JEDEC JESD84-B45 and the mechanical standard by JESD84-C44 (**www.jedec.org**)
- ***GBE MDI ("Gigabit Ethernet Medium Dependent Interface")*** This is defined by IEEE 802.3. The 1000Base-T operation over copper twisted pair cabling is defined by IEEE 802.3ab (**www.ieee.org**)
- ***HDMI Specification***, Version 1.3a, November 10, 2006 © 2006 Hitachi and other companies (**www.hdmi.org**)
- ***The I2C Specification,*** Version 2.1, January 2000, Philips Semiconductor (now NXP) (**www.nxp.com**)
- ***I2S Bus Specification,*** Feb. 1986 and Revised June 5, 1996, Philips Semiconductor (now NXP) (**www.nxp.com**)
- ***JTAG ("Joint Test Action Group")*** This is defined by IEEE 1149.1-2001 - IEEE Standard Test Access Port and Boundary Scan Architecture (**www.ieee.org**)
- ***PICMG® EEEP Embedded EEPROM Specification,*** Rev. 1.0, August 2010 (**www.picmg.org**)
- ***PCI Express Specifications*** (**www.pci-sig.org**)
- ***Serial ATA Revision 3.1***, July 18, 2011, Gold Revision, © Serial ATA International Organization (**www.sata-io.org**)
- ***SD Specifications Part 1 Physical Layer Simplified Specification,*** Version 3.01, May 18, 2010, © 2010 SD Group and SD Card Association ("Secure Digital") (**www.sdcard.org**)
- ***SPI Bus –*** "Serial Peripheral Interface" – de-facto serial interface standard defined by Motorola. A good description may be found on Wikipedia (**http://en.wikipedia.org/wiki/Serial_Peripheral_Interface_Bus**)
- ***USB Specifications*** (**www.usb.org**)

2. Module Overview

2.1 Form Factor Feature Summary

- Ultra compact size & greater reliability
  - Module size : 68mm x 68mm
  - PCB thickness : 2.0 mm
  - The maximum board layer : 12 layers
  - Solder crack resistance / Anti-distortion / Better signal quality

- 4 Board-to-board connectors
  - Connector : Panasonic B2B connector
    (AXK600337YG on module, AXK500137YG on carrier board)
  - Pin count : 4 x 100 pins
  - Connector mating force : 98N
  - Connector operating temperature range : -55˚C ~85˚C.
  - Oxidation resistance / Excellent electrical performance / Anti-vibration

- Module input voltage
  - Voltage range: + 5.0V to + 24V
  - Allows operation for 5.0V fixed DC supply
  - Single supply (no separate standby voltage)
  - Module power pins allow 6A max at +5V, or 30W max input power

- Low power design
  - 2 to 6W typical Module power draw during active operation
  - Fanless
  - Optional thermal solution

2.2 Function list Summary

The following table summarizes which functions can be performed by RTX 2.0 and its quantities.

Function		Min / Max
Display	24-bit LVDS	0 / 1
	24-bit TTL	0 / 1
	LCD Backlight	0 / 1
	LCD PWM	0 / 1
	eDisplay Port	0 / 1
	HDMI	0 / 1
Video	CSI0 / PCAM Hi, 7 bits	0 / 1
	CSI1 /.PCAM Lo, 10 bits	0 / 1
	PCAM Support	0 / 2
Communication	10/100/1000Mbps LAN	0 / 1
Storage	MMC, 11 bits	0 / 2
	SDIO	0 / 2
	SATA	0 / 1
Audio	I2S	0 / 1
I/O Interface	PCIe x 1 lane	0 / 2
	USB 2.0	1 / 1
	USB 3.0	0 / 1
	USB OTG	0 / 1
	GPIO	4 / 18
	UART	1 / 4 (4 wires)
	SPI	0 / 4
	CAN Bus	0 / 2
	I²C	1 / 5
	Reserved	0 / 9
	Keypad pins	0 / 8
	System Bus	0 / 1
System Management	CB Reset Module to Carrier Board	1 / 1
	System Reset (Carrier Board to Module)	1 / 1
	Boot Select (image select)	3 / 3
	WDT Out	1 / 1
	Power management pins	9 / 9
	Power input pins	12 / 12
	GND pins	98

3. Signal Descriptions

3.1 Signal Direction and Type Definitions

3.1.1 Pin Types

I Input to the Module

O Output from the Module

I/O Bi-directional input / output signal

OD Open drain output

3.1.2 Buffer Types

CMOS Logic input or output. Input thresholds and output levels may be 80% of supply rail for high side and 20% of the relevant supply rail for low side. Please refer to the CPU vendor datasheet for details.

PCIE PCI Express compatible differential signal. Please refer to the PCI Express Specification for details. PCIE transmit pins (Module outputs) shall be AC coupled on the Module. PCIE receive pins (Module inputs) shall be DC coupled on the RTX Module and shall be assumed to be AC coupled off-Module, close to the signal source. If the target PCI Express device resides on the Carrier Board, the Module PCIE receive lanes (target PCIE device transmit lanes) shall be AC coupled near the device on the Carrier Board. If the Carrier Board implements a PCIE slot, then these signals shall be AC coupled on the add-in card, not on the Carrier Board.

SATA SATA compatible differential signal. Please refer to the SATA Specification for details. All SATA signals shall be AC coupled on the Module.

USB USB 2.0 compatible differential signal. Please refer to the USB 2.0 Specification for details.

USB SS USB 3.0 compatible differential signal. Please refer to the USB 3.0 Specification for details.

REF Reference voltage output. May be sourced from a Module power plane.

PDS Pull-down strap. A Module output pin that is either tied to GND or is not connected. Used to signal Module capabilities to the Carrier Board.

Analog Inputs and Outputs used for LAN is analog signals.

Power Inputs used for power delivery to the Module electronics.

3.2 Display interface

3.2.1 Display- 18/24 bit Parallel LCD Data

The signals in the table below support the Parallel LCD interfaces.

Table 3.2.1: Parallel LCD Data Signals, Pin Types, and Descriptions

Parallel LCD Data Signal name	Pin Location	Pin Type	Pwr Rail / Tolerance	Description	Module Termination	Carrier Board Termination
TTL_R0	B4	O CMOS	3.3V / 3.3V	Parallel LCD red color date bit 0 18 bit display implementations leave the LS bits not connected		
TTL_R1	B6	O CMOS	3.3V / 3.3V	Parallel LCD red color date bit 1 18 bit display implementations leave the LS bits not connected		
TTL_R2	B8	O CMOS	3.3V / 3.3V	Parallel LCD red color date bit 2		
TTL_R3	B10	O CMOS	3.3V / 3.3V	Parallel LCD red color date bit 3		
TTL_R4	B12	O CMOS	3.3V / 3.3V	Parallel LCD red color date bit 4		
TTL_R5	B14	O CMOS	3.3V / 3.3V	Parallel LCD red color date bit 5		
TTL_R6	B16	O CMOS	3.3V / 3.3V	Parallel LCD red color date bit 6		
TTL_R7	B18	O CMOS	3.3V / 3.3V	Parallel LCD red color date bit 7		
TTL_G0	B22	O CMOS	3.3V / 3.3V	Parallel LCD green color date bit 018 bit display implementations leave the LS		

				bits not connected		
TTL_G1	B24	O CMOS	3.3V / 3.3V	Parallel LCD green color date bit 118 bit display implementations leave the LS bits not connected		
TTL_G2	B26	O CMOS	3.3V / 3.3V	Parallel LCD green color date bit 2		
TTL_G3	B28	O CMOS	3.3V / 3.3V	Parallel LCD green color date bit 3		
TTL_G4	B30	O CMOS	3.3V / 3.3V	Parallel LCD green color date bit 4		
TTL_G5	B32	O CMOS	3.3V / 3.3V	Parallel LCD green color date bit 5		
TTL_G6	B34	O CMOS	3.3V / 3.3V	Parallel LCD green color date bit 6		
TTL_G7	B36	O CMOS	3.3V / 3.3V	Parallel LCD green color date bit 7		
TTL_B0	B40	O CMOS	3.3V / 3.3V	Parallel LCD blue color date bit 0 18 bit display implementations leave the LS bits not connected		
TTL_B1	B42	O CMOS	3.3V / 3.3V	Parallel LCD blue color date bit 1 18 bit display implementations leave the LS bits not connected		
TTL_B2	B44	O CMOS	3.3V / 3.3V	Parallel LCD blue color date bit 2		
TTL_B3	B46	O CMOS	3.3V / 3.3V	Parallel LCD blue color date bit 3		
TTL_B4	B48	O CMOS	3.3V / 3.3V	Parallel LCD blue color date bit 4		
TTL_B5	B50	O CMOS	3.3V / 3.3V	Parallel LCD blue color date bit 5		
TTL_B6	B52	O CMOS	3.3V / 3.3V	Parallel LCD blue color date bit 6		

TTL_B7	B54	O CMOS	3.3V / 3.3V	Parallel LCD blue color date bit 7		
TTL_HSYNC	B11	O CMOS	3.3V / 3.3V	Horizontal Sync – high pulse indicates the start of a new horizontal display line		
TTL_VSYNC	B13	O CMOS	3.3V / 3.3V	Vertical Synch – high pulse indicates the start of a new display frame		
TTL_DE	B15	O CMOS	3.3V / 3.3V	Display Enable – signal is high during the active display line; low otherwise		
TTL_PCLK	B19	O CMOS	3.3V / 3.3V	Pixel clock – display data transitions on the positive clock edge		
TTL_VDD_EN	D17	O CMOS	3.3V / 3.3V	Parallel LCD panel power enable		
PANEL_BKLT_EN	D23	O CMOS	3.3V / 3.3V	panel backlight enable		
PANEL_BKLT_PWM	D25	O CMOS	3.3V / 3.3V	panel backlight brightness control, PWM signal		

3.2.2 Display- 18/24 bit LVDS LCD Single Channel

Low voltage differential signaling flat-panel interface. The Module pin-out allows one single channel display interface (1 pixel per clock) with up to 24 bit color. Includes panel backlight control and EDID support.

The LVDS channel and the control signals are pin shared with eDP signals. Refer to Section 3.2.3 'eDP - Embedded DisplayPort'

Table 3.2.2: LVDS Signals, Pin Types, and Descriptions

LVDS Signal name	Pin Location	Pin Type	Pwr Rail / Tolerance	Description	Module Termination	Carrier Board Termination
LVDS_D0+	D31	O LVDS		LVDS Channel differential positive data 0		

LVDS_D0-	D29	O LVDS		LVDS Channel differential negative data 0		
LVDS_D1+	D37	O LVDS		LVDS Channel differential positive data 1		
LVDS_D1-	D35	O LVDS		LVDS Channel differential negative data 1		
LVDS_D2+	D43	O LVDS		LVDS Channel differential positive data 2		
LVDS_D2-	D41	O LVDS		LVDS Channel differential negative data 2		
LVDS_D3+	D55	O LVDS		LVDS Channel differential positive data 3		
LVDS_D3-	D53	O LVDS		LVDS Channel differential negative data 3		
LVDS_CLK+	D49	O LVDS		LVDS Channel differential positive clock		
LVDS_CLK-	D47	O LVDS		LVDS Channel differential negative clock		
LVDS_VDD_EN	D19	O CMOS	3.3V / 3.3V	LVDS panel power enable		
PANEL_BKLT_EN	D23	O CMOS	3.3V / 3.3V	panel backlight enable		
PANEL_BKLT_PWM	D25	O CMOS	3.3V / 3.3V	panel backlight brightness control, PWM signal		
I2C2_CLK (LVDS_I2C_CLK)	D32	I/O OD CMOS	3.3V / 3.3V	I2C clock output for LVDS display use	*PU 2.2~4.7KΩ	
I2C2_DATA (LVDS_I2C_DAT)	D30	I/O OD CMOS	3.3V / 3.3V	I2C data line for LVDS display use	*PU 2.2~4.7KΩ	

Note: *Please refer to the IC vendor datasheet for detailed Termination.

3.2.2 3.2.3 Display- eDP (Embedded DisplayPort)

RTX Modules allow the LVDS channel signals to be alternatively used for eDP. The manner in which LVDS or eDP operation is chosen is vendor dependent.

Table 3.2.3: eDP Signals, Pin Types, and Descriptions

eDP Signal name	Pin Location	Pin Type	Pwr Rail / Tolerance	Description	Module Termination	Carrier Board Termination
EDP_TX0+	D31	O eDP		eDP true signal link lane 0		*AC coupled Capacitor 75~200nF
EDP_TX0-	D29	O eDP		eDP complement signal link lane 0		AC coupled Capacitor 75~200nF
EDP_TX1+	D37	O eDP		eDP true signal link lane 1		AC coupled Capacitor 75~200nF
EDP_TX1-	D35	O eDP		eDP complement signal link lane 1		AC coupled Capacitor 75~200nF
EDP_TX2+	D43	O eDP		eDP true signal link lane 2		AC coupled Capacitor 75~200nF
EDP_TX2-	D41	O eDP		eDP complement signal link lane 2		AC coupled Capacitor 75~200nF
EDP_TX3+	D55	O eDP		eDP true signal link lane 3		AC coupled Capacitor 75~200nF
EDP_TX3-	D53	O eDP		eDP complement signal link lane 3		AC coupled Capacitor 75~200nF
EDP_AUX+-	D49	O eDP		eDP true signal auxiliary channel		AC coupled Capacitor 75~200nF
EDP_AUX-	D47	O eDP		eDP complement signal auxiliary channel		AC coupled Capacitor 75~200nF

EDP VDD_EN	D19	O CMOS	3.3V / 3.3V	eDP power enable		
PANEL_BKLT_EN	D23	O CMOS	3.3V / 3.3V	Panel backlight enable		
PANEL_BKLT_PWM	D25	O CMOS	3.3V / 3.3V	Panel backlight brightness control, PWM signal		
EDP_HPD	D21	I CMOS	3.3V / 3.3V	eDP Hot Plug Detect pin	PD 100K	

Note: *Please refer to the IC vendor datasheet for detailed Termination.

3.2.3 3.2.4 eDP / LVDS LCD Pin Sharing

Requirements for LVDS or eDP selection

Module LVDS Channel / eDP **may** support any combination of LVDS and eDP.

Module LVDS Channel / eDP **may** support Dual Mode.

Module that support Dual-Mode **shall** implement the necessary muxing circuitry and control logic to ensure that the Module works properly with Carriers expecting either eDP or LVDS

Table 3.2.4: LVDS / eDP Pin Assignment

Pin Location	**LVDS**	**eDP**
D31	LVDS_D0+	EDP_TX0+
D29	LVDS_D0-	EDP_TX0-
D37	LVDS_D1+	EDP_TX1+
D35	LVDS_D1-	EDP_TX1-
D43	LVDS_D2+	EDP_TX2+
D41	LVDS_D2-	EDP_TX2-
D55	LVDS_D3+	EDP_TX3+
D53	LVDS_D3-	EDP_TX3-
D49	LVDS_CLK+	EDP_AUX+-
D47	LVDS_CLK-	EDP_AUX-
D19	LVDS_VDD_EN	EDP VDD_EN
D23	LVDS_BKLT_EN	EDP_BKLT_EN
D25	LVDS_BKLT_PWM	EDP_BKLT_PWM
D32	I2C2_CLK (LVDS_I2C_CK)	No use RSVD
D30	I2C2_DATA (LVDS_I2C_DAT)	No use RSVD

D21	No use	EDP_HPD

3.2.4 3.2.5 Display- HDMI

HDMI (High-Definition Multimedia Interface). The signals in the table below support the HDMI interfaces.

Table 3.2.5: HDMI Signals, Pin Types, and Descriptions

HDMI Signal name	Pin Location	Pin Type	Pwr Rail / Tolerance	Description	Module Termination	Carrier Board Termination
HDMI_D0+	D71	O TMDS		HDMI differential positive data 0		
HDMI_D0-	D73	O TMDS		HDMI differential negative data 0		
HDMI_D1+	D65	O TMDS		HDMI differential positive data 1		
HDMI_D1-	D67	O TMDS		HDMI differential negative data 1		
HDMI_D2+	D59	O TMDS		HDMI differential positive data 2		
HDMI_D2-	D61	O TMDS		HDMI differential negative data 2		
HDMI_CLK+	D77	O TMDS		HDMI differential positive data 3		
HDMI_CLK-	D79	O TMDS		HDMI differential negative data 3		
HDMI_DDC_SCL	D89	I/O OD CMOS	3.3V / 3.3V	I2C clock for HDMI use	*PU 2.2~4.7KΩ	
HDMI_DDC_SDA	D87	I/O OD CMOS	3.3V / 3.3V	I2C data for HDMI use	*PU 2.2~4.7KΩ	
HDMI_CEC	D83	I/O CMOS	3.3V / 3.3V	General Purpose 1-Wire bus interface. Can be used for consumer electronics control bus (CEC) of HDMI		
HDMI_HPD	D85	I CMOS	3.3V / 3.3V	HDMI Hot-Plug Detect	PD 100K (Without on Module)	

Note: *Please refer to the CPU vendor datasheet for detailed Termination.

3.3 Camera Interfaces

RTX Module support serial and parallel camera interfaces. The same pins are used for serial and parallel camera data interfaces, and a given design will generally be used with either serial camera(s) or parallel camera(s).

3.3.1 CSI (Serial Camera Input) Interface

CAM0 refers to the CSI0 pin group, pin shared with the high order PCAM bits, PCAM_D[10:15].

CAM1 refers to the CSI1 pin group, pin shared with the low order PCAM bits, PCAM_D[0:9].

Table 3.3.1: CSI Bus Signals, Pin Types, and Descriptions

CSI Bus Signal name	Pin Location	Pin Type	Pwr Rail / Tolerance	Description	Module Termination	Carrier Board Termination
CSI0_D0+	C12	I LVDS		CSI0 differential positive data 0 inputs Pin shared with parallel PCAM_ D12	*	
CSI0_D0-	C10	I LVDS		CSI0 differential negative data 0 inputs Pin shared with parallel PCAM_ D13		
CSI0_D1+	C6	I LVDS		CSI0 differential positive data 1 inputs Pin shared with parallel PCAM _D14		
CSI0_D1-	C4	I LVDS		CSI0 differential negative data 1 inputs Pin shared with parallel PCAM _D15		
CSI0_CK+	C18	I LVDS		CSI0 differential positive clock inputs Pin shared with parallel PCAM _D10		
CSI0_CK-	C16	I LVDS		CSI0 differential negative clock inputs Pin shared with parallel PCAM _D11		
CAM_MCK	C33	O CMOS	3.3V / 3.3V	Master clock output for CSI camera support (***may*** be used for CSI0 and / or CSI1)		
PCAM_ON_CSI0#	D94	O CMOS	3.3V / 3.3V	***Shall*** be tied to GND on the Module if the Module supports a parallel camera interface on the RTX CSI0 pin group ***Shall*** be an open pin on the Module if the Module supports a serial camera interface over the CSI0 pin group. Modules that do not use the CSI0 pin group ***may*** leave the PCAM_CSI0 pin		

				open.		
CAM0_PWR#	D96	O CMOS	3.3V / 3.3V	Camera 0 Power Enable, active low output.		
CAM0_RST#	D98	O CMOS	3.3V / 3.3V	Camera 0 Reset, active low output		
CSI1_D0+	C23	I LVDS		CSI1 differential positive data 0 inputs Pin shared with parallel PCAM _D2	*	
CSI1_D0-	C21	I LVDS		CSI0 differential negative data 0 inputs Pin shared with parallel PCAM _D3		
CSI1_D1+	C17	I LVDS		CSI0 differential positive data 1inputs Pin shared with parallel PCAM _D4		
CSI1_D1-	C15	I LVDS		CSI0 differential negative data 1 inputs Pin shared with parallel PCAM _D5		
CSI1_D2+	C11	I LVDS		CSI0 differential positive data 2inputs Pin shared with parallel PCAM _D6		
CSI1_D2-	C9	I LVDS		CSI0 differential negative data 2 inputs Pin shared with parallel PCAM _D7		
CSI1_D3+	C5	I LVDS		CSI0 differential positive data3 inputs Pin shared with parallel PCAM _D8		
CSI1_D3-	C3	I LVDS		CSI0 differential negative data 3 inputs Pin shared with parallel PCAM _D9		
CSI1_CK+	C29	I LVDS		CSI1 differential positive clock inputs Pin shared with parallel PCAM _D0		
CSI1_CK-	C27	I LVDS		CSI1 differential negative clock inputs Pin shared with parallel PCAM _D1		
PCAM_ON_CSI1#	D93	O CMOS	3.3V / 3.3V	***Shall*** be tied to GND on the Module if the Module supports a parallel camera interface on the RTX CSI1 pin group ***Shall*** be an open pin on the Module if the Module supports a serial camera interface over the CSI1 pin group. Modules that do not use the CSI1 pin group ***may*** leave the PCAM_CSI1 pin open.		
CAM1_PWR#	D95	O CMOS	3.3V / 3.3V	Camera 1 Power Enable, active low output.		

CAM1_RST#	D97	O CMOS	3.3V / 3.3V	Camera 1 Reset, active low output		

Note: Channel 1: 4 parallel, Channel 0: 2 parallel.

3.3.1 3.3.2 PCAM (Parallel Camera Input) Interface

Table 3.3.2: PCAM Bus Signals, Pin Types, and Descriptions

CSI Bus Signal name	**Pin Location**	**Pin Type**	**Pwr Rail / Tolerance**	**Description**	**Module Termination**	**Carrier Board Termination**
PCAM_D0	C29	I COMS	3.3V / 3.3V	Parallel camera input data, bits 0 Pin shared with CSI1_CK+ at CSI1 Interface		
PCAM_D1	C27	I COMS	3.3V / 3.3V	Parallel camera input data, bits 1 Pin shared with CSI1_CK- at CSI1 Interface		
PCAM_D2	C23	I COMS	3.3V / 3.3V	Parallel camera input data, bits 2 Pin shared with CSI1_D0+ at CSI1 Interface		
PCAM_D3	C21	I COMS	3.3V / 3.3V	Parallel camera input data, bits 3 Pin shared with CSI1_D0- at CSI1 Interface		
PCAM_D4	C17	I COMS	3.3V / 3.3V	Parallel camera input data, bits 4 Pin shared with CSI1_D1+ at CSI1 Interface		
PCAM_D5	C15	I COMS	3.3V / 3.3V	Parallel camera input data, bits 5 Pin shared with CSI1_D1- at CSI1 Interface		
PCAM_D6	C11	I COMS	3.3V / 3.3V	Parallel camera input data, bits 6 Pin shared with CSI1_D2+ at CSI1 Interface		
PCAM_D7	C9	I COMS	3.3V / 3.3V	Parallel camera input data, bits 7 Pin shared with CSI1_D2- at CSI1 Interface		
PCAM_D8	C5	I COMS	3.3V / 3.3V	Parallel camera input data, bits 8 Pin shared with CSI1_D3+ at CSI1 Interface		
PCAM_D9	C3	I COMS	3.3V / 3.3V	Parallel camera input data, bits 9 Pin shared with CSI1_D3- at CSI1		

				Interface		
PCAM_PXL_CK0	C37	I COMS	3.3V / 3.3V	Parallel camera primary pixel clock input		
PCAM_VSYNC	C28	I COMS	3.3V / 3.3V	Parallel camera Vertical Sync input		
PCAM_HSYNC	C26	I COMS	3.3V / 3.3V	Parallel camera Horizontal Sync input		
PCAM_DE	C30	I COMS	3.3V / 3.3V	Parallel camera Data Enable input		
PCAM_MCK	C22	O COMS	3.3V / 3.3V	Parallel camera Master Clock output		
PCAM_FLD	C32	I COMS	3.3V / 3.3V	Parallel camera Field input		
PCAM_ON_CSI1#	D93	O CMOS	3.3V / 3.3V	***Shall*** be tied to GND on the Module if the Module supports a parallel camera interface on the RTX CSI1 pin group. ***Shall*** be an open pin on the Module if the Module supports a serial camera interface over the CSI1 pin group. Modules that do not use the CSI1 pin group ***may*** leave the PCAM_CSI1 pin open.		
CAM1_PWR#	D95	O CMOS	3.3V / 3.3V	Camera 1 Power Enable, active low output.		
CAM1_RST#	D97	O CMOS	3.3V / 3.3V	Camera 1 Reset, active low output		
PCAM_D10	C18	I COMS	3.3V / 3.3V	Parallel camera input data, bits 10 Pin shared with CSI0_CK+at CSI0 Interface		
PCAM_D11	C16	I COMS	3.3V / 3.3V	Parallel camera input data, bits 11 Pin shared with CSI0_CK- at CSI0 Interface		
PCAM_D12	C12	I COMS	3.3V / 3.3V	Parallel camera input data, bits 12 Pin shared with CSI0_D0+ at CSI0 Interface		
PCAM_D13	C10	I COMS	3.3V / 3.3V	Parallel camera input data, bits 13 Pin shared with CSI0_D0+ at CSI0		

				Interface		
PCAM_D14	C6	I COMS	3.3V / 3.3V	Parallel camera input data, bits 14 Pin shared with CSI0_D1+ at CSI0 Interface		
PCAM_D15	C4	I COMS	3.3V / 3.3V	Parallel camera input data, bits 15 Pin shared with CSI0_D1+ at CSI0 Interface		
PCAM_PXL_CK1	C34	I COMS	3.3V / 3.3V	Parallel camera secondary pixel clock input – 2nd video parallel port (8 bit format with embedded synchs only)		
PCAM_ON_CSI0#	D94	O CMOS	3.3V / 3.3V	***Shall*** be tied to GND on the Module if the Module supports a parallel camera interface on the RTX CSI0 pin group. ***Shall*** be an open pin on the Module if the Module supports a serial camera interface over the CSI0 pin group. Modules that do not use the CSI0 pin group ***may*** leave the PCAM_CSI0 pin open.		
CAM0_PWR#	D96	O CMOS	3.3V / 3.3V	Camera 0 Power Enable, active low output.		
CAM0_RST#	D98	O CMOS	3.3V / 3.3V	Camera 0 Reset, active low output		

3.3.2 3.3.3 CSI / PCAM Pin Sharing

A pair of pins are defined on the Module to indicate to the Carrier what Camera interface(s) are supported by the Module. Carrier boards that implement parallel camera(s) logic ***shall*** decode these Camera Type pins. Such Carriers ***shall not*** power up a Carrier Camera interface that is incompatible with the Module implementation.

Table 3.3.3: CSI / PCAM Pin Assignment

Pin Location	CSI	PCAM
C29	CSI1_CK+	PCAM_D0
C27	CSI1_CK-	PCAM_D1
C23	CSI1_D0+	PCAM_D2
C21	CSI1_D0-	PCAM_D3

C17	CSI1_D1+	PCAM_D4
C15	CSI1_D1-	PCAM_D5
C11	CSI1_D2+	PCAM_D6
C9	CSI1_D2-	PCAM_D7
C5	CSI1_D3+	PCAM_D8
C3	CSI1_D3-	PCAM_D9
C18	CSI0_CK+	PCAM_D10
C16	CSI0_CK-	PCAM_D11
C12	CSI0_D0+	PCAM_D12
C10	CSI0_D0-	PCAM_D13
C6	CSI0_D1+	PCAM_D14
C4	CSI0_D1-	PCAM_D15

3.4 SDIO / SDMMC Interfaces

3.4.1 3.4.1 SDIO Card (4 bit) Interface

The Carrier SDIO Card ***may*** be selected as the Boot Device.

Table 3.4.1: SDIO Channel 0 Signals, Pin Types, and Descriptions

SDIO Signal name	Pin Location	Pin Type	Pwr Rail / Tolerance	Description	Module Termination	Carrier Board Termination
SD0_D0	B39	I/O CMOS	3.3V / 3.3V	SDIO Channel 0 Data bit0. These signals operates in push-pull mode		
SD0_D1	B41	I/O CMOS	3.3V / 3.3V	SDIO Channel 0 Data bit1. These signals operates in push-pull mode		
SD0_D2	B43	I/O CMOS	3.3V / 3.3V	SDIO Channel 0 Data bit2. These signals operates in push-pull mode		
SD0_D3	B45	I/O CMOS	3.3V / 3.3V	SDIO Channel 0 Data bit3. These signals operates in push-pull mode		
SD0_CLK	B47	O CMOS	3.3V / 3.3V	SDIO Channel 0 Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs. This signal has maximum frequency of 48MHz.		
SD0_CD#	B31	I CMOS	3.3V / 3.3V	SDIO Channel 0 Card Detect. This signal indicates when a SDIO/MMC	PU 10KΩ	

				card is present.		
SD0_WP	B33	I CMOS	3.3V / 3.3V	SDIO Channel 0 Write Protect. This signal denotes the state of the write-protect tab on SD cards.	PU 10KΩ	
SD0_CMD	B37	I/O CMOS	3.3V / 3.3V	SDIO Channel 0 Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode.	PU 10KΩ	
VDD_SD0_EN	B29	O CMOS	3.3V / 3.3V	Channel 0 SD card power enable		

3.4.2 3.4.2 e.MMC (8 bit) Interface

RTX Module pin definition allows for an 8 bit eMMC interface. However, with most SOCs, there will only be a single eMMC interface available from the SOC. If the SOC eMMC path is used for an on-Module boot device, then the interface **may not** be available to the Carrier.

If the SOC eMMC interface is not used on-Module, it **may** be available off-Module. In that case, Carrier eMMC Interface **may** be selected as the Boot Device

Table 3.4.2: SDIO Channel 1 Signals, Pin Types, and Descriptions

SDIO Signal name	Pin Location	Pin Type	Pwr Rail / Tolerance	Description	Module Termination	Carrier Board Termination
SD1_D0	B60	I/O CMOS	3.3V / 3.3V	SDIO Channel 1 Data bit0. These signals operates in push-pull mode		
SD1_D1	B62	I/O CMOS	3.3V / 3.3V	SDIO Channel 1 Data bit1. These signals operates in push-pull mode		
SD1_D2	B64	I/O CMOS	3.3V / 3.3V	SDIO Channel 1 Data bit2. These signals operates in push-pull mode		
SD1_D3	B66	I/O CMOS	3.3V / 3.3V	SDIO Channel 1 Data bit3. These signals operates in push-pull mode		
SD1_D4	B68	I/O CMOS	3.3V / 3.3V	SDIO Channel 1 Data bit4. These signals operates in push-pull mode		

SD1_D5	B70	I/O CMOS	3.3V / 3.3V	SDIO Channel 1 Data bit5. These signals operates in push-pull mode		
SD1_D6	B72	I/O CMOS	3.3V / 3.3V	SDIO Channel 1 Data bit6. These signals operates in push-pull mode		
SD1_D7	B74	I/O CMOS	3.3V / 3.3V	SDIO Channel 1 Data bit7. These signals operates in push-pull mode		
SD1_CLK	B76	O CMOS	3.3V / 3.3V	SDIO Channel 1 Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs. This signal has maximum frequency of 48 MHz.		
SD1_CD#	B53	I CMOS	3.3V / 3.3V	SDIO Channel 1 Card Detect. This signal indicates when a SDIO/MMC card is present.	*PU 10KΩ	
SD1_WP	B55	I CMOS	3.3V / 3.3V	SDIO Channel 1 Write Protect. This signal denotes the state of the write-protect tab on SD cards.	*PU 10KΩ	
SD1_CMD	B58	I/O CMOS	3.3V / 3.3V	SDIO Channel 1 Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode.	*PU 10KΩ	
VDD_SD1_EN	B51	O CMOS	3.3V / 3.3V	Channel 1 SD card power enable		

Note: *Please refer to the CPU vendor datasheet for detailed Termination. It needs to pull up 10k resistance if CPU did not support 10k resistance internally.

3.5 SPI Interface

Table 3.5: SPI Interface Signals, Pin Types, and Descriptions

SPI Signal name	Pin Location	Pin Type	Pwr Rail / Tolerance	Description	Module Termination	Carrier Board Termination
SPI0_MISO	B59	I CMOS	3.3V / 3.3V	SPI0 Master Data input from SPI device to SoC		

SPI0_MOSI	B61	O CMOS	3.3V / 3.3V	SPI0 Master Data output from SoC to SPI device		
SPI0_CS0#	B63	O CMOS	3.3V / 3.3V	SPI0 Master Chip Select 0 output		
SPI0_CS1#	B65	O CMOS	3.3V / 3.3V	SPI0 Master Chip Select 1 output		
SPI0_CLK	B67	O CMOS	3.3V / 3.3V	SPI0 Master Clock output		
SPI1_MISO	B71	I CMOS	3.3V / 3.3V	SPI1 Master Data input from SPI device to SoC		
SPI1_MOSI	B73	O CMOS	3.3V / 3.3V	SPI1 Master Data output from SoC to SPI device		
SPI1_CS0#	B75	O CMOS	3.3V / 3.3V	SPI1 Master Chip Select 0 output		
SPI1_CS1#	B77	O CMOS	3.3V / 3.3V	SPI1 Master Chip Select 1 output		
SPI1_CLK	B79	O CMOS	3.3V / 3.3V	SPI1 Master Clock output		

3.6 I2S Interfaces

I2S interfaces are defined one Port on RTX Module. That is typically used for digital audio I/O and other modest bandwidth functions. A common audio master clock signal is also defined.

Table 3.6: I2S Signals, Pin Types, and Descriptions

I2S Signal name	**Pin Location**	**Pin Type**	**Pwr Rail / Tolerance**	**Description**	**Module Termination**	**Carrier Board Termination**
I2S_BCLK	D46	I/O CMOS	3.3V / 3.3V	Digital audio clock		
I2S_DIN	D48	I CMOS	3.3V / 3.3V	Digital audio Input		
I2S_DOUT	D50	O CMOS	3.3V / 3.3V	Digital audio Output		
I2S_LRCLK	D52	I/O CMOS	3.3V / 3.3V	Left& Right audio synchronization clock		
I2S_MCLK	D54	O CMOS	3.3V / 3.3V	Master clock output to Audio codecs		

3.7 I2C Interface

RTX module support four channel I2C Bus.

Table 3.7: I2C Interface Signals, Pin Types, and Descriptions

I2C Signal name	Pin Location	Pin Type	Pwr Rail / Tolerance	Description	Module Termination	Carrier Board Termination
I2C0_DATA	D22	I/O OD CMOS	3.3V / 3.3V	I2C port 0 data line. Default used for Battery / RTC	* PU 2.2~4.7KΩ	
I2C0_CLK	D24	I/O OD CMOS	3.3V / 3.3V	I2C port 0 clock output. Default used for Battery / RTC	PU 2.2~4.7KΩ	
I2C1_DATA	D26	I/O OD CMOS	3.3V / 3.3V	I2C port 1 data line. Default used for CODEC / General purpose	PU 2.2~4.7KΩ	
I2C1_CLK	D28	I/O OD CMOS	3.3V / 3.3V	I2C port 1 clock output. Default used for CODEC / General purpose	PU 2.2~4.7KΩ	
I2C2_DATA	D30	I/O CMOS	3.3V / 3.3V	I2C port 2 data line. Default used for Camera / LVDS	PU 2.2~4.7KΩ	
I2C2_CLK	D32	I/O CMOS	3.3V / 3.3V	I2C port 2 clock output. Default used for Camera / LVDS	PU 2.2~4.7KΩ	
I2C3_DATA	B23	I/O CMOS	3.3V / 3.3V	I2C port 3 data line. Default used for TTL	PU 2.2~4.7KΩ	
I2C3_CLK	B25	I/O CMOS	3.3V / 3.3V	I2C port 3 clock output. Default used for TTL	PU 2.2~4.7KΩ	

Note: *Please refer to the IC vendor datasheet for detailed Termination.

3.8 Asynchronous Serial Ports (UART)

RTX Module pins for up to four asynchronous serial ports are defined. The ports are designated SER0 – SER3. Ports. All Ports are 4 wire ports (2 data lines and 2 handshake lines), also support 2 wire (data only).

Table 3.8: UART Signals, Pin Types, and Descriptions

UART Signal name	Pin Location	Pin Type	Pwr Rail / Tolerance	Description	Module Termination	Carrier Board Termination
UART0_TX	D58	O CMOS	3.3V / 3.3V	Asynchronous serial port 0 data out		
UART0_RX	D60	I CMOS	3.3V / 3.3V	Asynchronous serial port 0 data in	Note 1	
UART0_RTS#	D62	O CMOS	3.3V / 3.3V	Request to Send handshake line for UART0		
UART0_CTS#	D64	I CMOS	3.3V / 3.3V	Clear to Send handshake line for UART0	Note 1	
UART1_TX	D66	O CMOS	3.3V / 3.3V	Asynchronous serial port 1 data out		
UART1_RX	D68	I CMOS	3.3V / 3.3V	Asynchronous serial port 1 data in	Note 1	
UART1_RTS#	D70	O CMOS	3.3V / 3.3V	Request to Send handshake line for UART1		
UART1_CTS#	D72	I CMOS	3.3V / 3.3V	Clear to Send handshake line for UART1	Note 1	
UART2_TX	D76	O CMOS	3.3V / 3.3V	Asynchronous serial port 2 data out		
UART2_RX	D78	I CMOS	3.3V / 3.3V	Asynchronous serial port 2 data in	Note 1	
UART2_RTS#	D80	O CMOS	3.3V / 3.3V	Request to Send handshake line for UART2		
UART2_CTS#	D82	I CMOS	3.3V / 3.3V	Clear to Send handshake line for UART2	Note 1	
UART3_TX	D84	O CMOS	3.3V / 3.3V	Asynchronous serial port 3 data out		
UART3_RX	D86	I CMOS	3.3V / 3.3V	Asynchronous serial port 3 data in	Note 1	
UART3_RTS#	D88	O CMOS	3.3V / 3.3V	Request to Send handshake line for UART3		
UART3_CTS#	D90	I CMOS	3.3V / 3.3V	Clear to Send handshake line for UART3	Note 1	

Note 1. All other inputs should be weakly terminated to their inactive states.

3.9 CAN Bus Interface

Controller Area Network (CAN or CAN-bus) is a message based protocol designed specifically for automotive applications but now is also used in other areas such as industrial automation and medical equipment. RTX module support two channel CAN Bus.

Table 3.9: CAN Bus Signals, Pin Types, and Descriptions

CAN Bus Signal name	Pin Location	Pin Type	Pwr Rail / Tolerance	Description	Module Termination	Carrier Board Termination
CAN0_TX	D36	O CMOS	3.3V / 3.3V	TX output for CAN Bus channel 0		
CAN0_RX	D38	I CMOS	3.3V / 3.3V	RX input for CAN Bus channel 0		
CAN1_TX	D40	O CMOS	3.3V / 3.3V	TX output for CAN Bus channel 1		
CAN1_RX	D42	I CMOS	3.3V / 3.3V	RX input for CAN Bus channel 1		

3.10 USB Interfaces

3.10.1 3.10.1 USB 2.0 / 3.0

Table 3.10.1: USB 2.0 / 3.0 Signals, Pin Types, and Descriptions

USB Signal name	Pin Location	Pin Type	Pwr Rail / Tolerance	Description	Module Termination	Carrier Board Termination
USB_HOST_D+	C90	I/O USB		Differential USB 2.0 host positive data		
USB_HOST_D-	C92	I/O USB		Differential USB 2.0 host negative data		
USB_SS_TX+	C95	O USB SS		SuperSpeed transmitter differential positive data	AC coupled Capacitor 100nF	
USB_SS_TX-	C97	O USB SS		SuperSpeed transmitter differential negative data	AC coupled Capacitor 100nF	
USB_SS_RX+	C96	I USB		SuperSpeed receiver differential positive data	AC coupled Capacitor	

		SS			100nF	
USB_SS_RX-	C98	I USB SS		SuperSpeed receiver differential negative data	AC coupled Capacitor 100nF	
USB_HOST_OC#	C91	I CMOS	3.3V / 3.3V	USB host Port over-current sense.	PU 10KΩ	
USB_HOST_PWR_EN	C89	O CMO	3.3V / 3.3V	USB host port power enable		

3.10.2 3.10.2 USB OTG

Table 3.10.2: USB 2.0 OTG Signals, Pin Types, and Descriptions

USB OTG Signal name	**Pin Location**	**Pin Type**	**Pwr Rail / Tolerance**	**Description**	**Module Termination**	**Carrier Board Termination**
USB_OTG_D+	C84	I/O USB		Differential USB 2.0 OTG positive data.		
USB_OTG_D-	C86	I/O USB		Differential USB 2.0 OTG negative data		
USB_OTG_OC#	C76	I CMOS	3.3V / 3.3V	USB OTG port over-current sense.	PU 10 KΩ	
USB_OTG_ID	C78	I CMOS	3.3V / 3.3V	USB OTG ID input, active high.		
USB_OTG_VBUS_DET	C80	I CMOS	5V / USB VBUS 5V	USB host power detection, when this port is used as a device.		
USB_OTG_PWR_EN	C74	O CMOS	3.3V / 3.3V	USB OTG port power enable		

3.11PCI-express

The Module **may** implement up to two PCIe x1 links, designated PCIe Port 0, 1. The links **may** be PCIe Gen 1, 2 or 3, as the Module SoC allows.

The Module PCIe links are primarily PCIe Root Complexes. If the SoC allows it, the PCIe link(s) **may** alternatively be configured as a PCIe target(s). This is Module vendor specific.

3.11.1 3.11.1 PCI-express Port 0

Table 3.11.1: PCIe Port 0 Signals, Pin Types, and Descriptions

PCIe Signal name	Pin Location	Pin Type	Pwr Rail / Tolerance	Description	Module Termination	Carrier Board Termination
PCIE0_TX+	C41	O PCIe		Differential PCIe Port 0 transmit positive data	AC coupled Capacitor 100nF	
PCIE0_TX-	C43	O PCIe		Differential PCIe Port 0 transmit negative data	AC coupled Capacitor 100nF	
PCIE0_RX+	C47	I PCIe		Differential PCIe Port 0 receive positive data		
PCIE0_RX-	C49	I PCIe		Differential PCIe Port 0 receive negative data		
PCIE0_CLK+	C53	O PCIe		Differential PCIe Port 0 reference positive clock output	AC coupled Capacitor 100nF	
PCIE0_CLK-	C55	O PCIe		Differential PCIe Port 0 reference negative clock output	AC coupled Capacitor 100nF	
PCIE0_RST#	C61	O CMOS	3.3V / 3.3V	PCIe Port 0 reset output		
PCIE0_PWR_EN	C59	O CMOS	3.3V / 3.3V	PCIe Port 0 power enable		

3.11.2 3.11.2 PCI-express Port 1

Table 3.11.2: PCIe Port 1 Signals, Pin Types, and Descriptions

PCIe Signal name	Pin Location	Pin Type	Pwr Rail / Tolerance	Description	Module Termination	Carrier Board Termination
PCIE1_TX+	C38	O PCIe		Differential PCIe Port 1 transmit positive data	AC coupled Capacitor 100nF	
PCIE1_TX-	C40	O PCIe		Differential PCIe Port 1 transmit negative data	AC coupled Capacitor 100nF	

PCIE1_RX+	C44	I PCIe		Differential PCIe Port 1 receive positive data		
PCIE1_RX-	C46	I PCIe		Differential PCIe Port 1 receive negative data		
PCIE1_CLK+	C50	O PCIe		Differential PCIe Port 1 reference positive clock output	AC coupled Capacitor 100nF	
PCIE1_CLK-	C52	O PCIe		Differential PCIe Port 1 reference negative clock output	AC coupled Capacitor 100nF	
PCIE1_RST#	C58	O CMOS	3.3V / 3.3V	PCIe Port 1 reset output		
PCIE1_PWR_EN	C56	O CMOS	3.3V / 3.3V	PCIe Port 1 power enable		

3.11.3 3.11.3 PCI-express Wake Signal

Table 3.11.3: PCIe Wake Signals, Pin Types, and Descriptions

PCIe Signal name	Pin Location	Pin Type	Pwr Rail / Tolerance	Description	Module Termination	Carrier Board Termination
PCIE_WAKE#	C60	I CMOS	3.3V / 3.3V	PCIe wake up interrupt to host – common to PCIe Port 0, 1	PU 10KΩ	

3.12SATA

RTX Module definition allows for one SATA port. The port **may** be SATA Gen 1, 2 or 3 as the Module SoC allows.

The Carrier SATA device **may** be selected as the Boot Device

Table 3.12: SATA Signals, Pin Types, and Descriptions

SATA Signal name	Pin Location	Pin Type	Pwr Rail / Tolerance	Description	Module Termination	Carrier Board Termination
SATA_TX+	D3	O SATA		Differential SATA transmit positive data	*AC coupled Capacitor 100nF	
SATA_TX-	D5	O SATA		Differential SATA transmit negative data	*AC coupled Capacitor	

					100nF	
SATA_RX+	D9	I SATA		Differential SATA receive positive data	*AC coupled Capacitor 100nF	
SATA_RX-	D11	I SATA		Differential SATA receive negative data	*AC coupled Capacitor 100nF	
SATA_PWR_EN	D15	O CMOS	3.3V / 3.3V	SATA port power enable		

Note: *Please refer to the IC vendor datasheet for detailed AC coupled.

3.13System Bus (Extension Bus)

A system bus is a single computer bus that connects the major components of a computer system. The technique was developed to reduce costs and improve modularity. It combines the functions of a data bus to carry information, an address bus to determine where it should be sent, and a control bus to determine its operation. RTX support 16 bits data bus (Data 0~15) and 31 bits address bus (Address 0~30).

Table 3.13: System Bus Signals, Pin Types, and Descriptions

System Bus Signal name	Pin Location	Pin Type	Pwr Rail / Tolerance	Description	Module Termination	Carrier Board Termination
SYSBUS_A0	A21	O CMOS	3.3V / 3.3V	System Bus Address bit 0		
SYSBUS_A1	A23	O CMOS	3.3V / 3.3V	System Bus Address bit 1		
SYSBUS_A2	A25	O CMOS	3.3V / 3.3V	System Bus Address bit 2		
SYSBUS_A3	A27	O CMOS	3.3V / 3.3V	System Bus Address bit 3		
SYSBUS_A4	A29	O CMOS	3.3V / 3.3V	System Bus Address bit 4		
SYSBUS_A5	A31	O CMOS	3.3V / 3.3V	System Bus Address bit 5		
SYSBUS_A6	A33	O CMOS	3.3V / 3.3V	System Bus Address bit 6		

SYSBUS_A7	A35	O CMOS	3.3V / 3.3V	System Bus Address bit 7		
SYSBUS_A8	A22	O CMOS	3.3V / 3.3V	System Bus Address bit 8		
SYSBUS_A9	A24	O CMOS	3.3V / 3.3V	System Bus Address bit 9		
SYSBUS_A10	A26	O CMOS	3.3V / 3.3V	System Bus Address bit 10		
SYSBUS_A11	A28	O CMOS	3.3V / 3.3V	System Bus Address bit 11		
SYSBUS_A12	A30	O CMOS	3.3V / 3.3V	System Bus Address bit 12		
SYSBUS_A13	A32	O CMOS	3.3V / 3.3V	System Bus Address bit 13		
SYSBUS_A14	A34	O CMOS	3.3V / 3.3V	System Bus Address bit 14		
SYSBUS_A15	A36	O CMOS	3.3V / 3.3V	System Bus Address bit 15		
SYSBUS_A16	A39	O CMOS	3.3V / 3.3V	System Bus Address bit 16		
SYSBUS_A17	A41	O CMOS	3.3V / 3.3V	System Bus Address bit 17		
SYSBUS_A18	A43	O CMOS	3.3V / 3.3V	System Bus Address bit 18		
SYSBUS_A19	A45	O CMOS	3.3V / 3.3V	System Bus Address bit 19		
SYSBUS_A20	A47	O CMOS	3.3V / 3.3V	System Bus Address bit 20		
SYSBUS_A21	A49	O CMOS	3.3V / 3.3V	System Bus Address bit 21		
SYSBUS_A22	A51	O CMOS	3.3V / 3.3V	System Bus Address bit 22		
SYSBUS_A23	A53	O CMOS	3.3V / 3.3V	System Bus Address bit 23		
SYSBUS_A24	A40	O CMOS	3.3V / 3.3V	System Bus Address bit 24		
SYSBUS_A25	A42	O CMOS	3.3V / 3.3V	System Bus Address bit 25		

SYSBUS_A26	A44	O CMOS	3.3V / 3.3V	System Bus Address bit 26		
SYSBUS_A27	A46	O CMOS	3.3V / 3.3V	System Bus Address bit 27		
SYSBUS_A28	A48	O CMOS	3.3V / 3.3V	System Bus Address bit 28		
SYSBUS_A29	A50	O CMOS	3.3V / 3.3V	System Bus Address bit 29		
SYSBUS_A30	A52	O CMOS	3.3V / 3.3V	System Bus Address bit 30		
SYSBUS_D0	A3	I/O CMOS	3.3V / 3.3V	System Bus Data bit 0		
SYSBUS_D1	A5	I/O CMOS	3.3V / 3.3V	System Bus Data bit 1		
SYSBUS_D2	A7	I/O CMOS	3.3V / 3.3V	System Bus Data bit 2		
SYSBUS_D3	A9	I/O CMOS	3.3V / 3.3V	System Bus Data bit 3		
SYSBUS_D4	A11	I/O CMOS	3.3V / 3.3V	System Bus Data bit 4		
SYSBUS_D5	A13	I/O CMOS	3.3V / 3.3V	System Bus Data bit 5		
SYSBUS_D6	A15	I/O CMOS	3.3V / 3.3V	System Bus Data bit 6		
SYSBUS_D7	A17	I/O CMOS	3.3V / 3.3V	System Bus Data bit 7		
SYSBUS_D8	A4	I/O CMOS	3.3V / 3.3V	System Bus Data bit 8		
SYSBUS_D9	A6	I/O CMOS	3.3V / 3.3V	System Bus Data bit 9		
SYSBUS_D10	A8	I/O CMOS	3.3V / 3.3V	System Bus Data bit 10		
SYSBUS_D11	A10	I/O CMOS	3.3V / 3.3V	System Bus Data bit 11		
SYSBUS_D12	A12	I/O CMOS	3.3V / 3.3V	System Bus Data bit 12		
SYSBUS_D13	A14	I/O CMOS	3.3V / 3.3V	System Bus Data bit 13		

SYSBUS_D14	A16	I/O CMOS	3.3V / 3.3V	System Bus Data bit 14		
SYSBUS_D15	A18	I/O CMOS	3.3V / 3.3V	System Bus Data bit 15		
SYSBUS_BE0#	A65	O CMOS	3.3V / 3.3V	System Bus Byte Enable 0		
SYSBUS_BE1#	A67	O CMOS	3.3V / 3.3V	System Bus Byte Enable 1		
SYSBUS_CLK	A72	O CMOS	3.3V / 3.3V	System Bus Clock Output		
SYSBUS_WE#	A69	O CMOS	3.3V / 3.3V	System Bus Write Enable		
SYSBUS_OE#	A71	O CMOS	3.3V / 3.3V	System Bus Output Enable		
SYSBUS_WAIT#	A64	I CMOS	3.3V / 3.3V	System Bus Wait		
SYSBUS_CS0#	A66	O CMOS	3.3V / 3.3V	System Bus Chip Select 0		
SYSBUS_CS1#	A68	O CMOS	3.3V / 3.3V	System Bus Chip Select 1		
SYSBUS_ALE	A63	O CMOS	3.3V / 3.3V	System Bus Address Latch Enable		
SYSBUS_INT0	A57	I CMOS	3.3V / 3.3V	System Bus Interrupt 0		
SYSBUS_INT1	A59	I CMOS	3.3V / 3.3V	System Bus Interrupt 1		
SYSBUS_INT2	A58	I CMOS	3.3V / 3.3V	System Bus Interrupt 2		
SYSBUS_INT3	A60	I CMOS	3.3V / 3.3V	System Bus Interrupt 3		

3.14GBE

Gigabit Ethernet ports may operate in 10, 100, or 1000 Mbit/sec modes. RTX Module shall implement one Ethernet port on the GBE port pin slot and this should be capable of at least 10/100 mode. Magnetics are assumed to be on the Carrier Board.

Table 3.14: Gigabit Ethernet Signals, Pin Types, and Descriptions

Gigabit Ethernet Signal name	Pin Location	Pin Type	Pwr Rail / Tolerance	Description	Module Termination	Carrier Board Termination
GBE_MDI0+	C65	I/O Analog		Gigabit Ethernet Media Dependent Interface Differential Pairs 0 positive data		
GBE_MDI0-	C67	I/O Analog		Gigabit Ethernet Media Dependent Interface Differential Pairs 0 negative data		
GBE_MDI1+	C71	I/O Analog		Gigabit Ethernet Media Dependent Interface Differential Pairs 1 positive data		
GBE_MDI1-	C73	I/O Analog		Gigabit Ethernet Media Dependent Interface Differential Pairs 1 negative data		
GBE_MDI2+	C77	I/O Analog		Gigabit Ethernet Media Dependent Interface Differential Pairs 2 positive data		
GBE_MDI2-	C79	I/O Analog		Gigabit Ethernet Media Dependent Interface Differential Pairs 2 negative data		
GBE_MDI3+	C83	I/O Analog		Gigabit Ethernet Media Dependent Interface Differential Pairs 3 positive data		
GBE_MDI3-	C85	I/O Analog		Gigabit Ethernet Media Dependent Interface Differential Pairs 3 negative data		
GBE_XFMR_VREF	C64	REF	GND~3.3V	Reference voltage for Carrier Board Ethernet Controller magnetics center tap. The reference voltage is determined by the requirements of the Module PHY and may be as low as 0V and as high as 3.3V. The reference voltage output ***shall*** be current limited on the Module. In the case in which the reference is shorted to ground, the current ***shall*** be		

				limited to 250 mA or less.		
GBE_LINK_ACT#	C66	OD CMOS	3.3V / 3.3V	Gigabit Ethernet Controller activity indicator, active low. ***Shall*** be able to sink 24mA or more Carrier LED current.		
GBE_LINK100#	C68	OD CMOS	3.3V / 3.3V	Gigabit Ethernet Controller 100 Mbit / sec link indicator, active low. ***Shall*** be able to sink 24mA or more Carrier LED current.		
GBE_LINK1000#	C70	OD CMOS	3.3V / 3.3V	Gigabit Ethernet Controller 1000 Mbit / sec link indicator, active low. ***Shall*** be able to sink 24mA or more Carrier LED current.		

3.15GPIO

3.15.1 3.15.1 GPIO Interface

Table 3.15.1: GPIO Signals, Pin Types, and Descriptions

GPIO Signal name	Pin Location	Pin Type	Pwr Rail / Tolerance	Description	Module Termination	Carrier Board Termination
GPIO0	B80	I/O CMOS	3.3V / 3.3V	general purpose input / output 0 Default setting is GPO		
GPIO1	B82	I/O CMOS	3.3V / 3.3V	general purpose input / output 1 Default setting is GPO		
GPIO2	B84	I/O CMOS	3.3V / 3.3V	general purpose input / output 2 Default setting is GPO		
GPIO3	B86	I/O CMOS	3.3V / 3.3V	general purpose input / output 3 Default setting is GPO		
GPIO4	B88	I/O CMOS	3.3V / 3.3V	general purpose input / output 4 Default setting is GPO		
GPIO5	B90	I/O CMOS	3.3V / 3.3V	general purpose input / output 5 Default setting is GPI		
GPIO6	B92	I/O CMOS	3.3V / 3.3V	general purpose input / output 6 Default setting is GPI		
GPIO7	B94	I/O CMOS	3.3V / 3.3V	general purpose input / output 7 Default setting is GPI		

GPIO8	B96	I/O CMOS	3.3V / 3.3V	general purpose input / output 8 Default setting is GPI		
GPIO9	B98	I/O CMOS	3.3V / 3.3V	General purpose input / output 9 Default setting is GPI		
GPIO10	B83	I/O CMOS	3.3V / 3.3V	general purpose input / output 10 multi-function pin with Keypad COL0 Default setting is Keypad COL0		
GPIO11	B85	I/O CMOS	3.3V / 3.3V	general purpose input / output 11 multi-function pin with Keypad COL1 Default setting is Keypad COL1		
GPIO12	B87	I/O CMOS	3.3V / 3.3V	general purpose input / output 12 multi-function pin with Keypad COL2 Default setting is Keypad COL2		
GPIO13	B89	I/O CMOS	3.3V / 3.3V	general purpose input / output 13 multi-function pin with Keypad COL3 Default setting is Keypad COL3		
GPIO14	B91	I/O CMOS	3.3V / 3.3V	general purpose input / output 14 multi-function pin with Keypad ROW0 Default setting is Keypad ROW0		
GPIO15	B93	I/O CMOS	3.3V / 3.3V	general purpose input / output 15 multi-function pin with Keypad ROW1 Default setting is Keypad ROW1		
GPIO16	B95	I/O CMOS	3.3V / 3.3V	general purpose input / output 16 multi-function pin with Keypad ROW2 Default setting is Keypad ROW2		
GPIO17	B97	I/O CMOS	3.3V / 3.3V	general purpose input / output 17 multi-function pin with Keypad ROW3 Default setting is Keypad ROW3		

3.15.2 3.15.2 GPIO Multi-Function Pin Sharing

Table 3.15.2: GPIO multi-function Pin Assignment

Pin Location	GPIO Signal	Multi-Function with
B83	GPIO10	Keypad COL0
B85	GPIO11	Keypad COL1
B87	GPIO12	Keypad COL2
B89	GPIO13	Keypad COL3
B91	GPIO14	Keypad ROW0

B93	GPIO15	Keypad ROW1
B95	GPIO16	Keypad ROW2
B97	GPIO17	Keypad ROW3

3.16Keypad

RTX Module support 4x4 Matrix (4 COL x 4 ROW) Keypad Function. The Interface is pin sharing with GPIO 14~17.

Table 3.16: Keypad Signals, Pin Types, and Descriptions

Keypad Signal name	Pin Location	Pin Type	Pwr Rail / Tolerance	Description	Module Termination	Carrier Board Termination
COL0	B83	I CMOS	3.3V / 3.3V	Keypad Interface COL0 multi-function pin with GPIO10		
COL1	B85	I CMOS	3.3V / 3.3V	Keypad Interface COL1 multi-function pin with GPIO11		
COL2	B87	I CMOS	3.3V / 3.3V	Keypad Interface COL2 multi-function pin with GPIO12		
COL3	B89	I CMOS	3.3V / 3.3V	Keypad Interface COL3 multi-function pin with GPIO13		
ROW0	B91	I CMOS	3.3V / 3.3V	Keypad Interface ROW0 multi-function pin with GPIO14		
ROW1	B93	I CMOS	3.3V / 3.3V	Keypad Interface ROW1 multi-function pin with GPIO15		
ROW2	B95	I CMOS	3.3V / 3.3V	Keypad Interface ROW2 multi-function pin with GPIO16		
ROW3	B97	I CMOS	3.3V / 3.3V	Keypad Interface ROW3 multi-function pin with GPIO17		

3.17 Boot select

Three Module pins allow the Carrier board user to select from eight possible boot devices. Three are Module devices, and four are Carrier devices, and one is a remote device. The pins ***shall*** be weakly pulled up on the Module and the pin states decoded by Module logic. The Carrier ***shall*** either leave the Module pin Not Connected (“Float” in the table below) or ***shall*** pull the pin to GND, per the second table below.

3.17.1 Boot Select Interface

Table 3.17.1: Boot Select Signals, Pin Types, and Descriptions

Boot Select Signal name	Pin Location	Pin Type	Pwr Rail / Tolerance	Description	Module Termination	Carrier Board Termination
BOOT_SEL0#	B3	I CMOS	3.3V / 3.3V	Input straps bit0 determine the Module boot device. Driven by OD part on Carrier.	PU 10KΩ	
BOOT_SEL1#	B5	I CMOS	3.3V / 3.3V	Input straps bit1 determine the Module boot device. Driven by OD part on Carrier.	PU 10KΩ	
BOOT_SEL2#	B7	I CMOS	3.3V / 3.3V	Input straps bit2 determine the Module boot device. Driven by OD part on Carrier.	PU 10KΩ	

3.17.2 Boot device selection

The definition of “boot” is left to the Module designer. Some designs may literally implement some or all of the table above, such that the first off-SOC code fetches come from the devices listed above. Alternatively, some designs may always fetch the first few off-SOC instructions from a fixed device, likely a SPI Flash EEPROM, and then re-direct the execution to another device per the table below.

Table 3.17.2: Boot device Selection

BOOT_SEL2#	BOOT_SEL1#	BOOT_SEL0#	Boot Source
GND	GND	GND	Carrier SATA
GND	GND	Float	Carrier SD Card
GND	Float	GND	Carrier eMMC Flash
GND	Float	Float	Carrier SPI
Float	GND	GND	Module device (NAND, NOR) – vendor specific
Float	GND	Float	Remote boot (GBE, serial) – vendor specific
Float	Float	GND	Module eMMC
Float	Float	Float	Module SPI

3.18 Management Pins

Table 3.18: Management Signals, Pin Types, and Descriptions

Management Pin Signal name	Pin Location	Pin Type	Pwr Rail / Tolerance	Description	Module Termination	Carrier Board Termination
POWER_BTN#	A84	I CMOS	3.3V / 3.3V	Power-button input from Carrier board. Carrier to float the line in in-active state. Active low, level sensitive. Should be de-bounced on the Module	*PU 10KΩ	
CB_PWR_EN	A77	O CMOS	3.3V / 3.3V	Carrier board circuits (apart from power management and power path circuits) should not be powered up until the Module asserts the CB_PWR_EN signal.		
CB_PGOOD	A79	I CMOS	3.3V / 3.3V	Carrier board power good indication from Carrier board. When CB_PWR_EN asserts Carrier system power rail (ex. 3.3V, 5V .. on Carrier board). All system power are ready on Carrier Board. CB_PGOOD asserts to Module.		
VCC_OK	A81	I CMOS	3.3V / 3.3V	RTX VCC Power Good indication from Carrier board. Module and Carrier power supplies (other than Module and Carrier power supervisory circuits) ***shall not*** be enabled while this signal is held low by the Carrier.		
RESET_IN#	A73	I CMOS	3.3V / 3.3V	Reset input from Carrier board. Carrier drives low to force a Module reset, floats the line otherwise.	*PU 10KΩ	
RESET_OUT#	A75	O CMOS	3.3V / 3.3V	General purpose reset output to Carrier board.		
SUSPEND_REQ#	A80	O CMOS	3.3V / 3.3V	The Module ***shall*** drive this signal low when the system is in a standby power state		
WAKE#	A76	I CMOS	3.3V / 3.3V	Wake indicator from Carrier board. ***May*** be sourced from user Wake button or Carrier logic. Carrier to float the line in	*PU 10KΩ	

				in-active state. Active low, level sensitive. ***Should*** be de-bounced on the Module.		
SLEEP#	A78	I CMOS	3.3V / 3.3V	Sleep indicator from Carrier board. ***May*** be sourced from user Sleep button or Carrier logic. Carrier to float the line in in-active state. Active low, level sensitive. ***Should*** be de-bounced on the Module.	*PU 10KΩ	
WDT_OUT#	A82	O CMOS	3.3V / 3.3V	General purpose Watchdog output to Carrier board.		

Note: *Please refer to the IC vendor datasheet for detailed Termination.

3.19Power & GND

Table 3.19.1: Power / GND, Pin Types, and Descriptions

Power / GND Signal name	**Pin Location**	**Pwr Rail / Tolerance**	**Description**
VCC	See Table 3.21.2	Power In	Module power input voltage – 4.75V min to 24V max
Ground	See Table 3.21.2	Ground	Module signal and power return, and GND reference
RTC_PWR	See Table 3.21.2	Power In	Low current RTC circuit backup power – 3.0V nominal May be sourced from a Carrier based Lithium cell or Super Cap.

Table 3.21.2: Power / GND pin Location

Power / GND	Pin Location
VCC	A87, A88, A89, A90, A91,A92, A93, A94, A95, A96, A97, A98
GND	A1, A2, A19, A20, A37, A38 A55, A56, A61, A62, A70, A74, A85, A86, A99, A100 B1, B2, B9, B17, B20, B21, B27, B35, B38, B49, B56, B57, B69, B78, B81, B99, B100 C1, C2, C7, C8, C13, C14, C19, C20, C24, C25, C31, C35, C36, C39, C42, C45, C48, C51, C54, C57,C62, C63, C69,C72,C75, C81, C82, C87, C88, C93, C94, C99, C100 D1, D2, D7, D13, D20, D27, D33, D34, D39, D44, D45, D51, D56, D57, D63, D69, D74, D75, D81, D91, D92, D99, D100
RTC_PWR	A83

4. Module Pin-Out Map

4.1 ROM Board to Board Connecter Pin-Out Map

4.1.1 Connector X1 Pin-Out Map

Odd number	RTX V2.0a	Pin Type	Even number	RTX V2.0a	Pin Type
A1	GND	PWR	A2	GND	PWR
A3	SYSBUS_D0	I/O	A4	SYSBUS_D8	I/O
A5	SYSBUS_D1	I/O	A6	SYSBUS_D9	I/O
A7	SYSBUS_D2	I/O	A8	SYSBUS_D10	I/O
A9	SYSBUS_D3	I/O	A10	SYSBUS_D11	I/O
A11	SYSBUS_D4	I/O	A12	SYSBUS_D12	I/O
A13	SYSBUS_D5	I/O	A14	SYSBUS_D13	I/O
A15	SYSBUS_D6	I/O	A16	SYSBUS_D14	I/O
A17	SYSBUS_D7	I/O	A18	SYSBUS_D15	I/O
A19	GND	PWR	A20	GND	PWR
A21	SYSBUS_A0	O	A22	SYSBUS_A8	O
A23	SYSBUS_A1	O	A24	SYSBUS_A9	O
A25	SYSBUS_A2	O	A26	SYSBUS_A10	O
A27	SYSBUS_A3	O	A28	SYSBUS_A11	O
A29	SYSBUS_A4	O	A30	SYSBUS_A12	O
A31	SYSBUS_A5	O	A32	SYSBUS_A13	O
A33	SYSBUS_A6	O	A34	SYSBUS_A14	O
A35	SYSBUS_A7	O	A36	SYSBUS_A15	O
A37	GND	PWR	A38	GND	PWR
A39	SYSBUS_A16	O	A40	SYSBUS_A24	O
A41	SYSBUS_A17	O	A42	SYSBUS_A25	O
A43	SYSBUS_A18	O	A44	SYSBUS_A26	O
A45	SYSBUS_A19	O	A46	SYSBUS_A27	O
A47	SYSBUS_A20	O	A48	SYSBUS_A28	O
A49	SYSBUS_A21	O	A50	SYSBUS_A29	O
A51	SYSBUS_A22	O	A52	SYSBUS_A30	O
A53	SYSBUS_A23	O	A54	RSVD	
A55	GND	PWR	A56	GND	PWR
A57	SYSBUS_INT0	I	A58	SYSBUS_INT2	I
A59	SYSBUS_INT1	I	A60	SYSBUS_INT3	I
A61	GND	PWR	A62	GND	PWR

A63	SYSBUS_ALE	O	A64	SYSBUS_WAIT#	I
A65	SYSBUS_BE0#	O	A66	SYSBUS_CS0#	O
A67	SYSBUS_BE1#	O	A68	SYSBUS_CS1#	O
A69	SYSBUS_WE#	O	A70	GND	PWR
A71	SYSBUS_OE#	O	A72	SYSBUS_CLK	O
A73	RESET_IN#	I/PU	A74	GND	PWR
A75	RESET_OUT#	O	A76	WAKE#	I/PU
A77	CB_PWR_EN	O	A78	SLEEP#	I/PU
A79	CB_PGOOD	I/PU	A80	SUSPEND_REQ#	O
A81	VCC_OK	I/PU	A82	WDT_OUT#	O
A83	RTC_PWR	PWR	A84	POWER_BTN#	I/PU
A85	GND	PWR	A86	GND	PWR
A87	VCC	PWR	A88	VCC	PWR
A89	VCC	PWR	A90	VCC	PWR
A91	VCC	PWR	A92	VCC	PWR
A93	VCC	PWR	A94	VCC	PWR
A95	VCC	PWR	A96	VCC	PWR
A97	VCC	PWR	A98	VCC	PWR
A99	GND	PWR	A100	GND	PWR

4.1.2 Connector X2 Pin-Out Map

Odd number	RTX V2.0a	Pin Type	Even number	RTX V2.0a	Pin Type
B1	GND	PWR	B2	GND	PWR
B3	BOOT_SEL0#	I/PU	B4	TTL_R0	O
B5	BOOT_SEL1#	I/PU	B6	TTL_R1	O
B7	BOOT_SEL2#	I/PU	B8	TTL_R2	O
B9	GND	PWR	B10	TTL_R3	O
B11	TTL_HSYNC	O	B12	TTL_R4	O
B13	TTL_VSYNC	O	B14	TTL_R5	O
B15	TTL_DE	O	B16	TTL_R6	O
B17	GND	PWR	B18	TTL_R7	O
B19	TTL_PCLK	O	B20	GND	PWR
B21	GND	PWR	B22	TTL_G0	O
B23	I2C3_DATA(for TTL)	I/O OD/PU	B24	TTL_G1	O
B25	I2C3_CLK(for TTL)	I/O OD/PU	B26	TTL_G2	O

B27	GND	PWR	B28	TTL_G3	O
B29	VDD_SD0_EN	O	B30	TTL_G4	O
B31	SD0_CD#	I/PU	B32	TTL_G5	O
B33	SD0_WP	I/PU	B34	TTL_G6	O
B35	GND	PWR	B36	TTL_G7	O
B37	SD0_CMD	I/O	B38	GND	PWR
B39	SD0_D0	I/O	B40	TTL_B0	O
B41	SD0_D1	I/O	B42	TTL_B1	O
B43	SD0_D2	I/O	B44	TTL_B2	O
B45	SD0_D3	I/O	B46	TTL_B3	O
B47	SD0_CLK	O	B48	TTL_B4	O
B49	GND	PWR	B50	TTL_B5	O
B51	VDD_SD1_EN	O	B52	TTL_B6	O
B53	SD1_CD#	I/PU	B54	TTL_B7	O
B55	SD1_WP	I/PU	B56	GND	PWR
B57	GND	PWR	B58	SD1_CMD	I/O
B59	SPI0_MISO	I	B60	SD1_D0	I/O
B61	SPI0_MOSI	O	B62	SD1_D1	I/O
B63	SPI0_CS0#	O	B64	SD1_D2	I/O
B65	SPI0_CS1#	O	B66	SD1_D3	I/O
B67	SPI0_CLK	O	B68	SD1_D4	I/O
B69	GND	PWR	B70	SD1_D5	I/O
B71	SPI1_MISO	I	B72	SD1_D6	I/O
B73	SPI1_MOSI	O	B74	SD1_D7	I/O
B75	SPI1_CS0#	O	B76	SD1_CLK	O
B77	SPI1_CS1#	O	B78	GND	PWR
B79	SPI1_CLK	O	B80	GPIO0	I/O /O
B81	GND	PWR	B82	GPIO1	I/O /O
B83	GPIO10/COL0	I/O /I	B84	GPIO2	I/O /O
B85	GPIO11/COL1	I/O /I	B86	GPIO3	I/O /O
B87	GPIO12/COL2	I/O /I	B88	GPIO4	I/O /O
B89	GPIO13/COL3	I/O /I	B90	GPIO5	I/O /I
B91	GPIO14/ROW0	I/O /I	B92	GPIO6	I/O /I
B93	GPIO15/ROW1	I/O /I	B94	GPIO7	I/O /I
B95	GPIO16/ROW2	I/O /I	B96	GPIO8	I/O /I
B97	GPIO17/ROW3	I/O /I	B98	GPIO9	I/O /I
B99	GND	PWR	B100	GND	PWR

4.1.3 Connector X3 Pin-Out Map

Odd number	RTX V2.0a	Pin Type	Even number	RTX V2.0a	Pin Type
C1	GND	PWR	C2	GND	PWR
C3	CSI1_D3- / PCAM_D9	DP/I	C4	CSI0_D1- / PCAM_D15	DP/I
C5	CSI1_D3+ / PCAM_D8	DP/I	C6	CSI0_D1+ / PCAM_D14	DP/I
C7	GND	PWR	C8	GND	PWR
C9	CSI1_D2- / PCAM_D7	DP/I	C10	CSI0_D0- / PCAM_D13	DP/I
C11	CSI1_D2+ / PCAM_D6	DP/I	C12	CSI0_D0+ / PCAM_D12	DP/I
C13	GND	PWR	C14	GND	PWR
C15	CSI1_D1- / PCAM_D5	DP/I	C16	CSI0_CK- / PCAM_D11	DP/I
C17	CSI1_D1+ / PCAM_D4	DP/I	C18	CSI0_CK+ / PCAM_D10	DP/I
C19	GND	PWR	C20	GND	PWR
C21	CSI1_D0- / PCAM_D3	DP/I	C22	PCAM_MCK	O
C23	CSI1_D0+ / PCAM_D2	DP/I	C24	GND	PWR
C25	GND	PWR	C26	PCAM_HSYNC	I
C27	CSI1_CK- / PCAM_D1	DP/I	C28	PCAM_VSYNC	I
C29	CSI1_CK+ / PCAM_D0	DP/I	C30	PCAM_DE	I
C31	GND	PWR	C32	PCAM_FLD	I
C33	CAM_MCK	O	C34	PCAM_PXL_CK1	I
C35	GND	PWR	C36	GND	PWR
C37	PCAM_PXL_CK0	I	C38	PCIE1_TX+	DP
C39	GND	PWR	C40	PCIE1_TX-	DP
C41	PCIE0_TX+	DP	C42	GND	PWR
C43	PCIE0_TX-	DP	C44	PCIE1_RX+	DP
C45	GND	PWR	C46	PCIE1_RX-	DP
C47	PCIE0_RX+	DP	C48	GND	PWR
C49	PCIE0_RX-	DP	C50	PCIE1_CLK+	DP
C51	GND	PWR	C52	PCIE1_CLK-	DP
C53	PCIE0_CLK+	DP	C54	GND	PWR
C55	PCIE0_CLK-	DP	C56	PCIE1_PWR_EN	O
C57	GND	PWR	C58	PCIE1_RST#	O
C59	PCIE0_PWR_EN	O	C60	PCIE_WAKE#	I/PU
C61	PCIE0_RST#	O	C62	GND	PWR
C63	GND	PWR	C64	GBE_XFMR_VREF	PWR
C65	GBE_MDI0+	DP	C66	GBE_LINK_ACT#	OD
C67	GBE_MDI0-	DP	C68	GBE_LINK100#	OD

C69	GND	PWR	C70	GBE_LINK1000#	OD
C71	GBE_MDI1+	DP	C72	GND	PWR
C73	GBE_MDI1-	DP	C74	USB_OTG_PWR_EN	O
C75	GND	PWR	C76	USB_OTG_OC#	I/PU
C77	GBE_MDI2+	DP	C78	USB_OTG_ID	I
C79	GBE_MDI2-	DP	C80	USB_OTG_VBUS_DET	I
C81	GND	PWR	C82	GND	PWR
C83	GBE_MDI3+	DP	C84	USB_OTG_D+	DP
C85	GBE_MDI3-	DP	C86	USB_OTG_D-	DP
C87	GND	PWR	C88	GND	PWR
C89	USB_HOST_PWR_EN	O	C90	USB_HOST_D+	DP
C91	USB_HOST_OC#	I/PU	C92	USB_HOST_D-	DP
C93	GND	PWR	C94	GND	PWR
C95	USB_SS_TX+	DP	C96	USB_SS_RX+	DP
C97	USB_SS_TX-	DP	C98	USB_SS_RX-	DP
C99	GND	PWR	C100	GND	PWR

4.1.4 Connector X4 Pin-Out Map

Odd number	RTX V2.0a	Pin Type	Even number	RTX V2.0a	Pin Type
D1	GND	PWR	D2	GND	PWR
D3	SATA_TX+	DP	D4	RSVD	
D5	SATA_TX-	DP	D6	RSVD	
D7	GND	PWR	D8	RSVD	
D9	SATA_RX+	DP	D10	RSVD	
D11	SATA_RX-	DP	D12	RSVD	
D13	GND	PWR	D14	RSVD	
D15	SATA_PWR_EN	O	D16	RSVD	
D17	TTL_VDD_EN	O	D18	RSVD	
D19	LCD_VDD_EN / EDP VDD_EN	O	D20	GND	PWR
D21	EDP_HPD	I/PD	D22	I2C0_DATA (for Battery / RTC)	I/O OD/PU
D23	PANEL_BKLT_EN	O	D24	I2C0_CLK (for Battery / RTC)	I/O OD/PU
D25	PANEL_BKLT_PWM	O	D26	I2C1_DATA (for CODEC)	I/O OD/PU
D27	GND	PWR	D28	I2C1_CLK (for CODEC)	I/O OD/PU
D29	LVDS_D0- / EDP_TX0-	DP	D30	I2C2_DATA(for Camera/LVDS)	I/O OD/PU
D31	LVDS_D0+ / EDP_TX0+	DP	D32	I2C2_CLK(for Camera/LVDS)	I/O OD/PU
D33	GND	PWR	D34	GND	PWR

D35	LVDS_D1- / EDP_TX1-	DP	D36	CAN0_TX	O
D37	LVDS_D1+ / EDP_TX1+	DP	D38	CAN0_RX	I
D39	GND	PWR	D40	CAN1_TX	O
D41	LVDS_D2- / EDP_TX2-	DP	D42	CAN1_RX	I
D43	LVDS_D2+ / EDP_TX2+	DP	D44	GND	PWR
D45	GND	PWR	D46	I2S_BCLK	I/O
D47	LVDS_CLK- / EDP_AUX-	DP	D48	I2S_DIN	I
D49	LVDS_CLK+ / EDP_AUX+	DP	D50	I2S_DOUT	O
D51	GND	PWR	D52	I2S_LRCLK	I/O
D53	LVDS_D3- / EDP_TX3-	DP	D54	I2S_MCLK	O
D55	LVDS_D3+ / EDP_TX3+	DP	D56	GND	PWR
D57	GND	PWR	D58	UART0_TX	O
D59	HDMI_D2+	DP	D60	UART0_RX	I
D61	HDMI_D2-	DP	D62	UART0_RTS#	O
D63	GND	PWR	D64	UART0_CTS#	I
D65	HDMI_D1+	DP	D66	UART1_TX	O
D67	HDMI_D1-	DP	D68	UART1_RX	I
D69	GND	PWR	D70	UART1_RTS#	O
D71	HDMI_D0+	DP	D72	UART1_CTS#	I
D73	HDMI_D0-	DP	D74	GND	PWR
D75	GND	PWR	D76	UART2_TX	O
D77	HDMI_CK+	DP	D78	UART2_RX	I
D79	HDMI_CK-	DP	D80	UART2_RTS#	O
D81	GND	PWR	D82	UART2_CTS#	I
D83	HDMI_CEC	I/O	D84	UART3_TX	O
D85	HDMI_HPD	I	D86	UART3_RX	I
D87	HDMI_DDC_SDA	I/O OD/PU	D88	UART3_RTS#	O
D89	HDMI_DDC_SCL	I/O OD/PU	D90	UART3_CTS#	I
D91	GND	PWR	D92	GND	PWR
D93	PCAM_ON_CSI1#	O	D94	PCAM_ON_CSI0#	O
D95	CAM1_PWR#	O	D96	CAM0_PWR#	O
D97	CAM1_RST#	O	D98	CAM0_RST#	O
D99	GND	PWR	D100	GND	PWR

5. Mechanical definitions

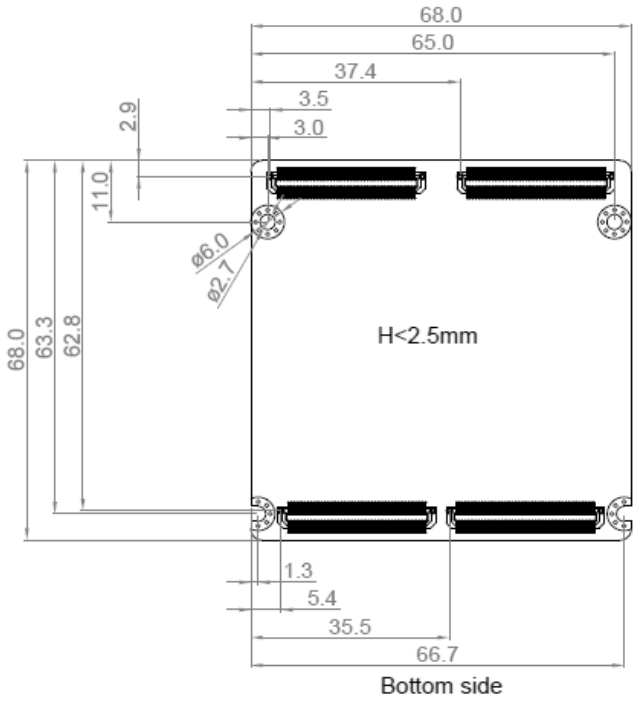
5.1 Carrier Connector

The Carrier board connector is 100pins Panasonic (AXK500137YG) board-to board connectors.

5.2 Module outline

The figure on the following page details the 68mmx68mm Module mechanical attributes.

Figure 68mm x68mm Module Outline



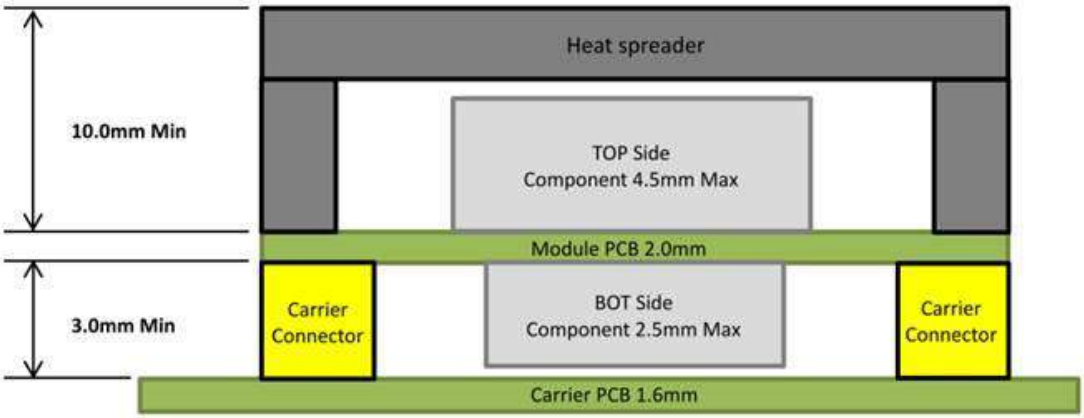
5.3 Module " Z " Height Considerations

Note from *the Module Outline* above that the component height on the Module is restricted to a maximum component height of 4.5 mm on the Module Primary (Top) side and to 2.5 mm on the Module Secondary (Bottom) side.

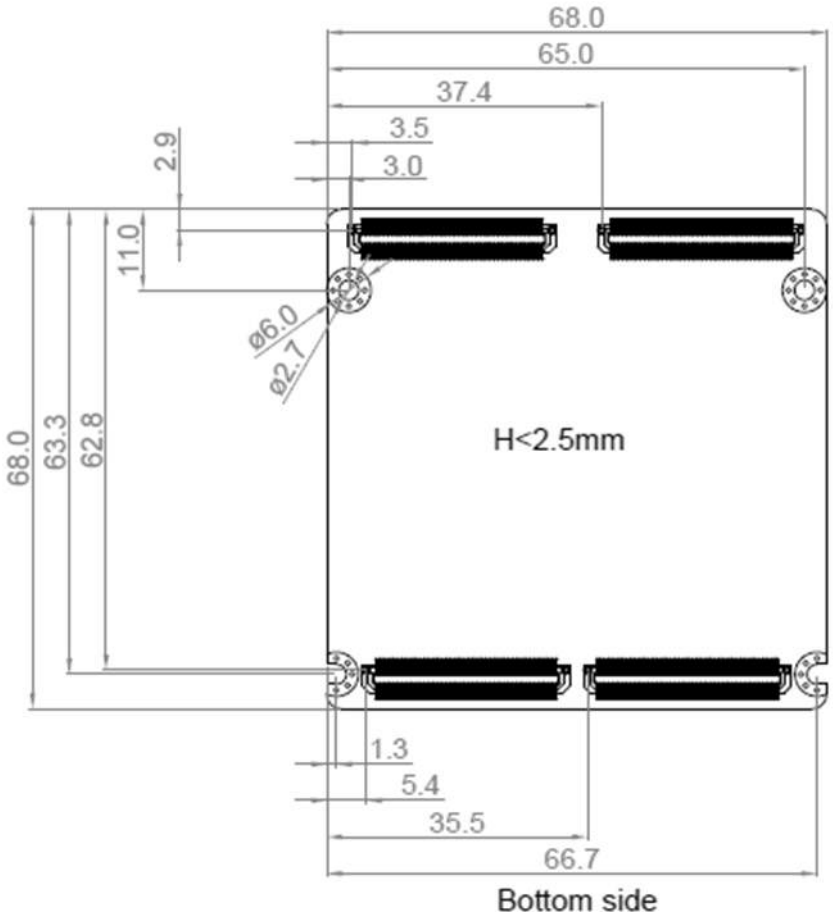
The 2.5mm Secondary side component height restriction allows the Module to be used with 2.5 mm stack-height Carrier connectors. When used with 2.5 mm stack height connectors, the 'Z' height profile from Carrier board Top side to tallest Module component is 15.0 mm.

When a 2.5mm stack height Carrier board connector is used, there *shall not* be components on the Carrier board Top side in the Module region. Additionally, when 2.5mm stack height connectors are used, there *should not* be PCB traces on the Carrier top side in the Module shadow. This is to prevent possible problems with metallic Module heat sink attachment hardware that may protrude through the Module.

Not shown in the figure below are any thermal dissipation components (heat sinks) nor is fastening hardware (standoffs, spacers, screws, washers, etc) shown. The dimensions of those components must of course be considered in a system design.



5.4 Carrier Board Connector PCB Footprint



5.5 Module and Carrier Board Mounting Holes – GND Connection

It ***shall*** be possible to tie all Module and Carrier board mounting holes to GND. The holes ***should*** be tied directly to the GND planes, although Module and Carrier designers ***may*** optionally make the mounting hole GND connections through passive parts, allowing the mounting holes to be isolated from GND if they feel it necessary.

5.6 Carrier Board Standoff

Standoffs secured to the Carrier board are expected. The standoffs are to be used with M2.5 hardware. Most implementations will use Carrier board standoffs that have M2.5 threads (as opposed to clearance holes). A short M2.5 screw and washer, inserted from the Module top side, secures the Module to the Carrier board threaded standoff.