

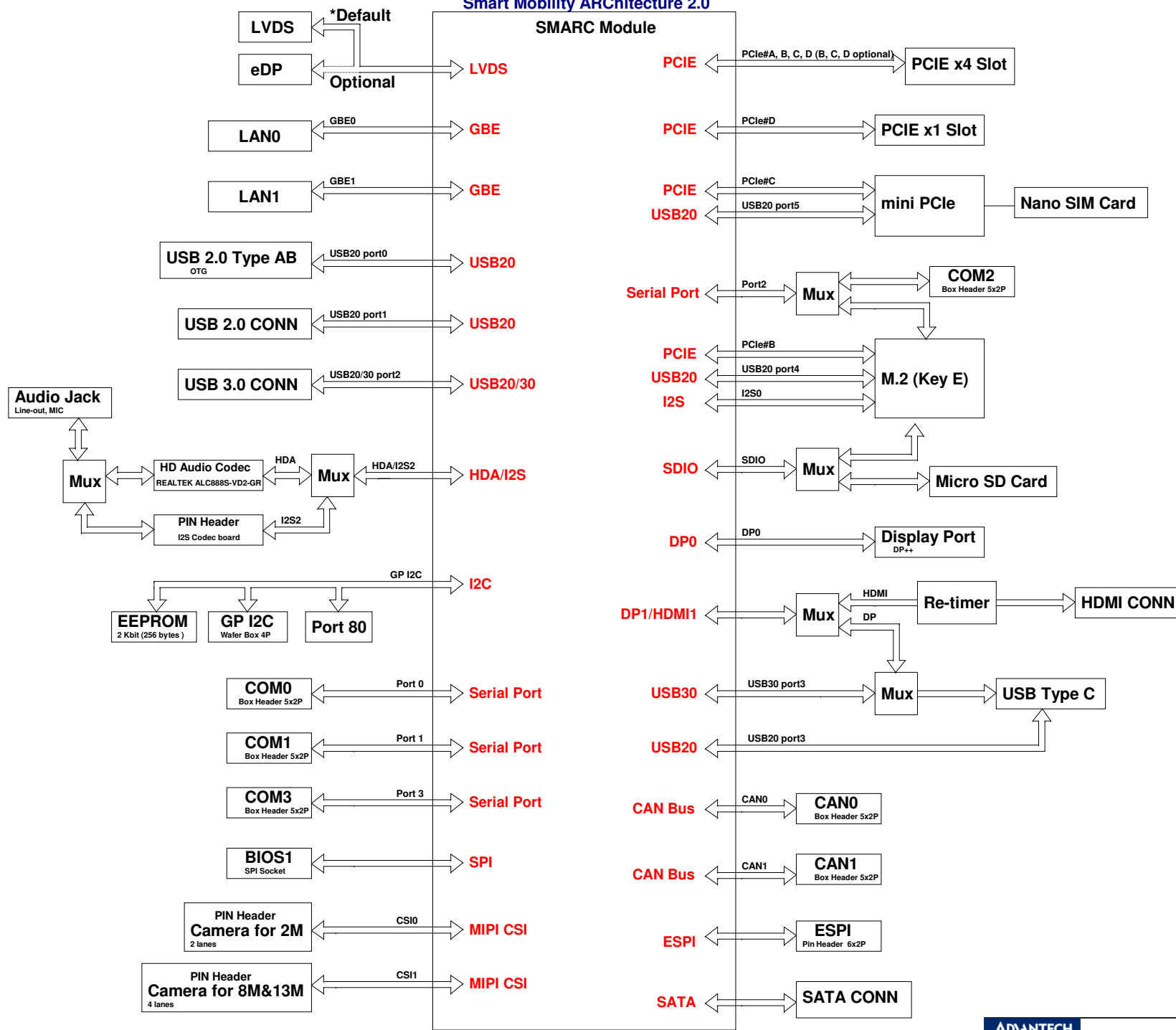
Model Name: SOM-DB2500

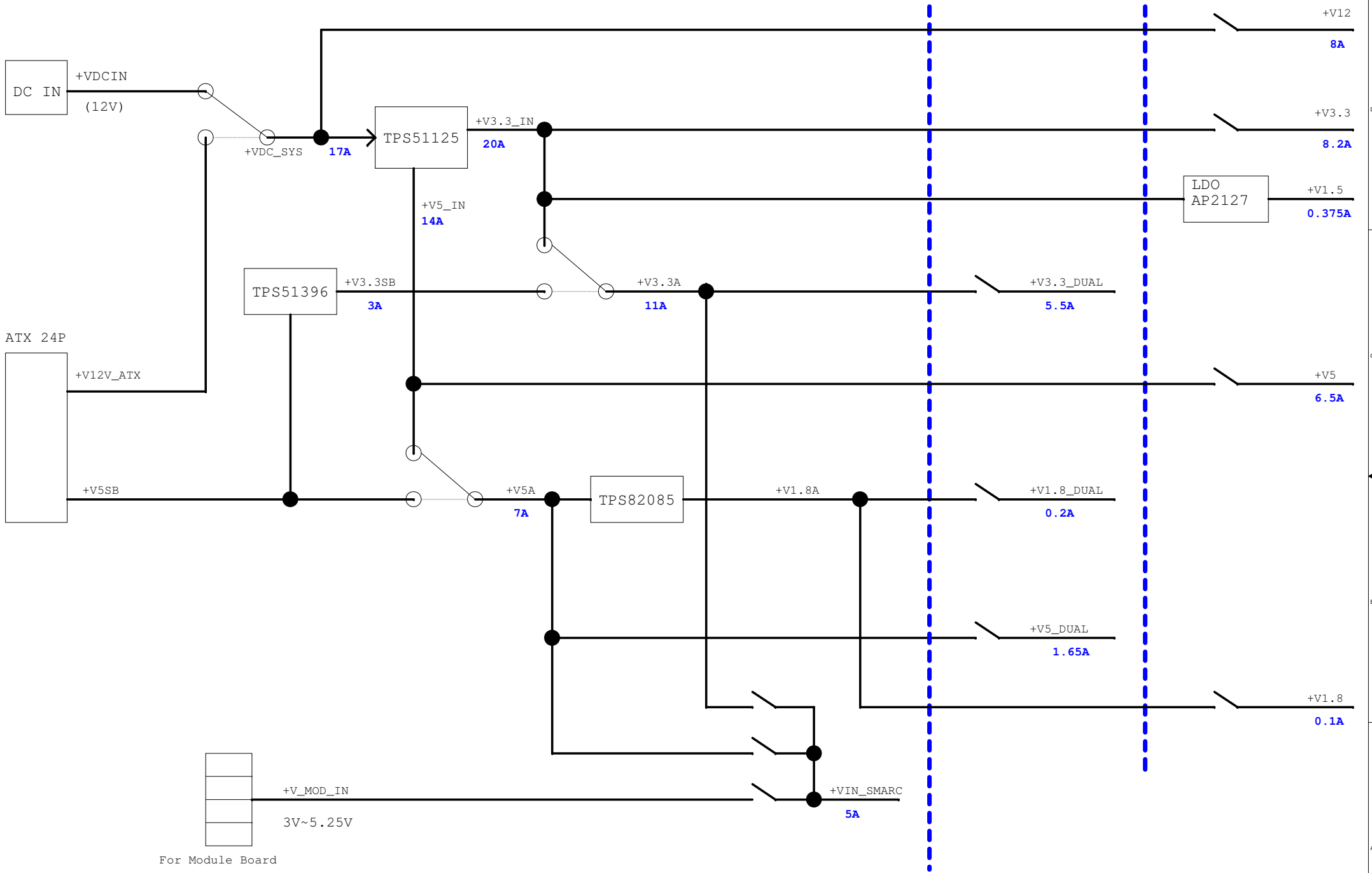
01	COVER
02	Block Diagram
03	Power Map
04	SMARC GF
05	USB Type C
06	LVDS Connecotor
07	PCIE X4 slot
08	Mini PCIE / M.2 (key E)
09	PCIE CLK BUF/PCIE X1 slot
10	HDA / I2S
11	Audio JACK
12	DP0 for DP++
13	DP1/HDMI1
14	BIOS socket/SATA/RTC
15	COM port
16	CAN BUS/eSPI/I2C
17	SDCARD/Boot SEL/GPIO
18	USB20/30 OTG
19	GBE X2 / MIPI CSI
20	FAN / Port 80
21	Level shifter
22	LED/SCREW/PROBE/BTN/PCB
23	DC / ATX

24	+V5A/+V3.3A
25	+V5_IN/+V3.3_IN
26	Suspend Power Rail
27	Core power rail
28	Module power path
29	Function Diagram
30	HDMI Re-Timer

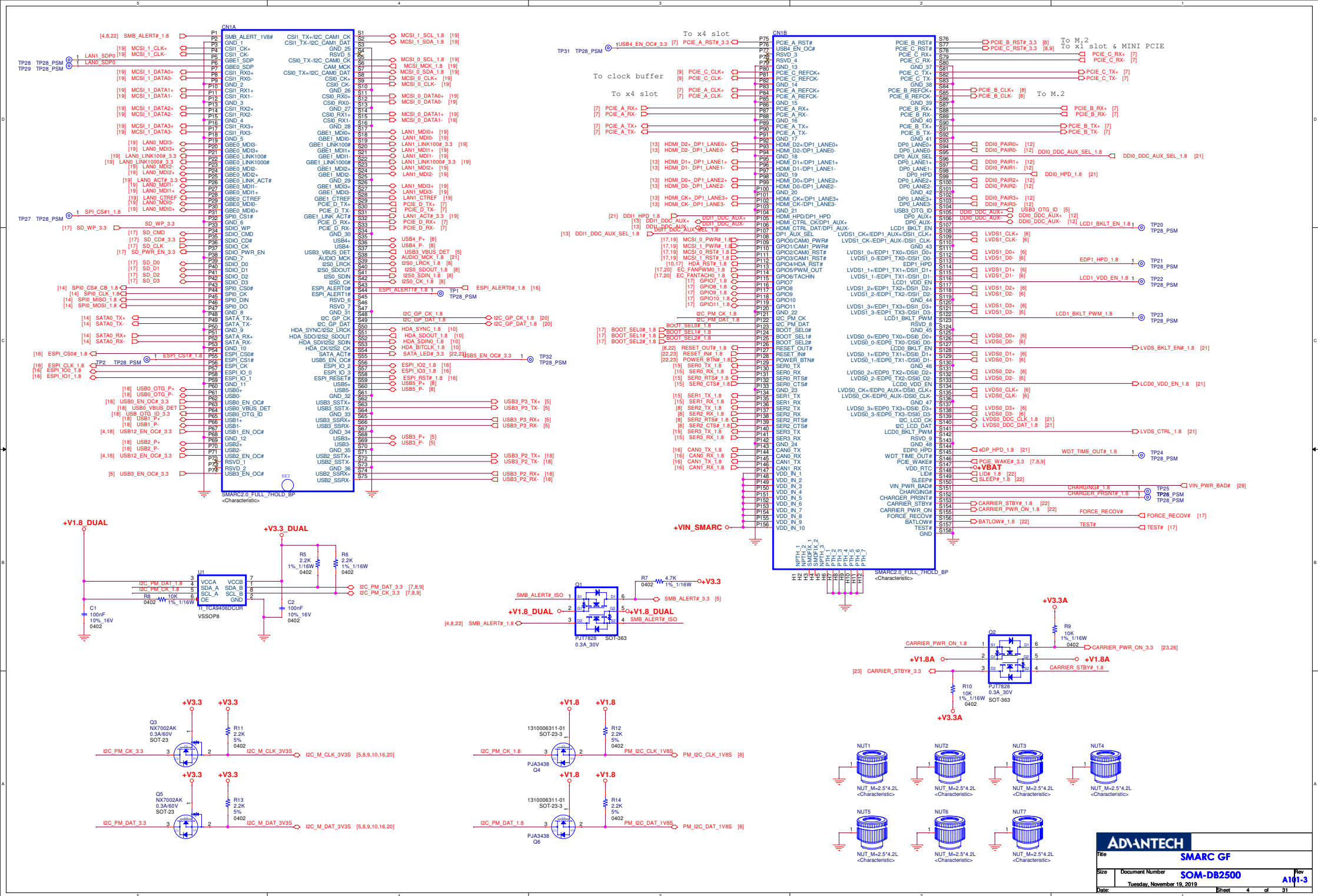
Smart Mobility ARChitecture 2.0

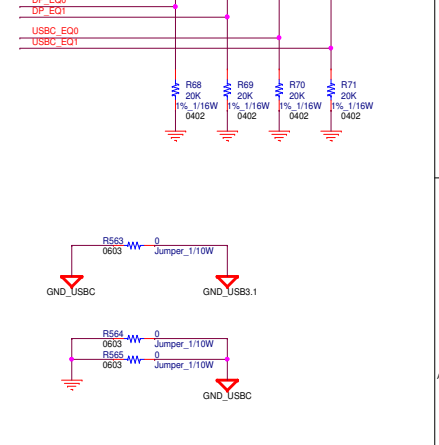
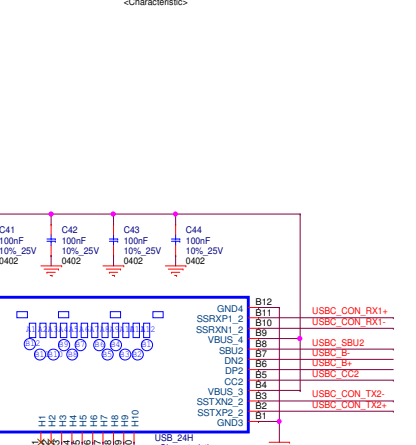
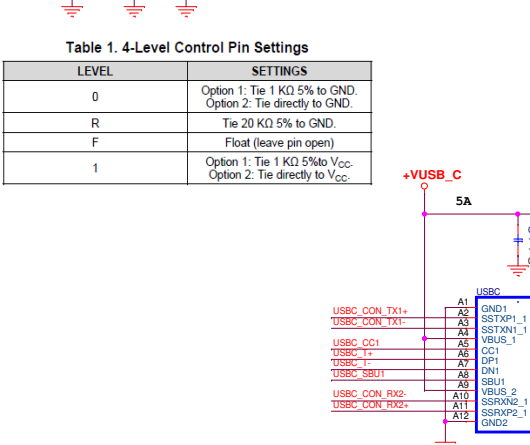
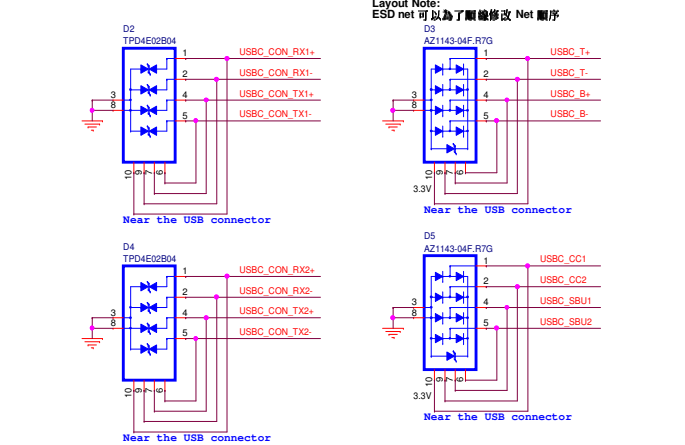
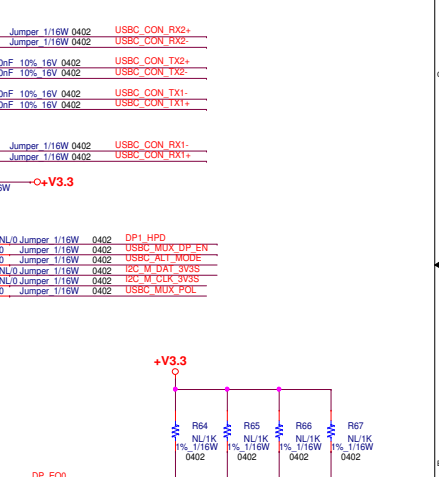
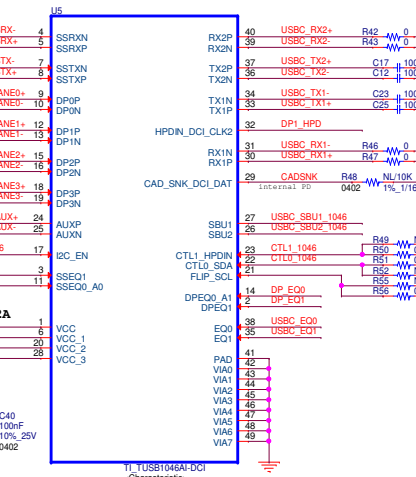
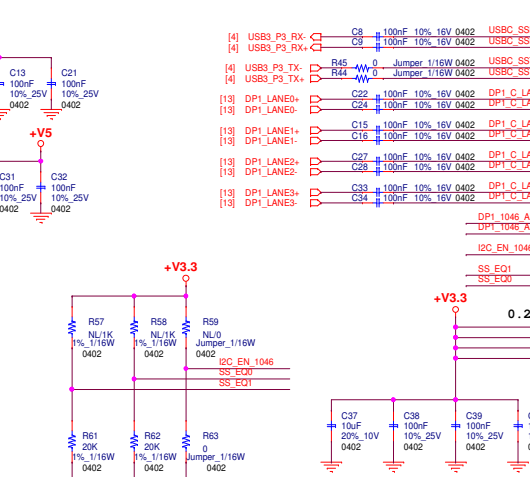
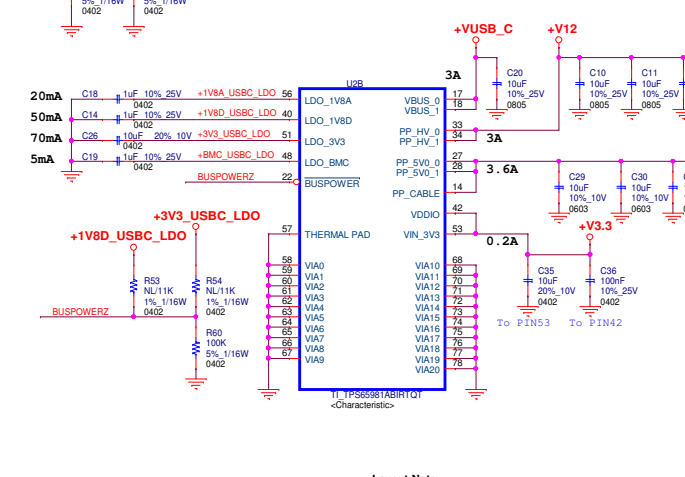
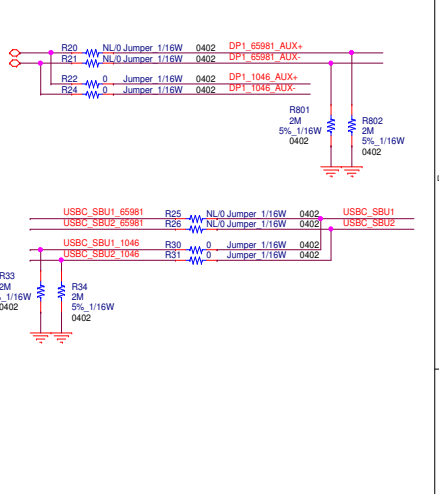
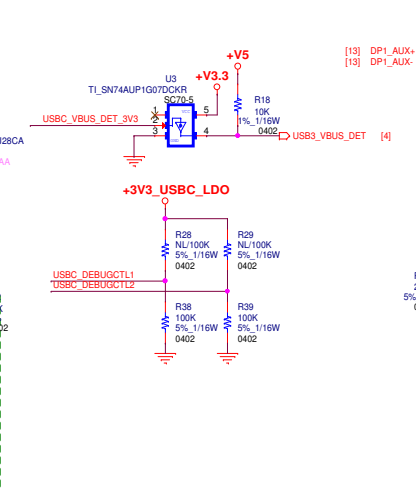
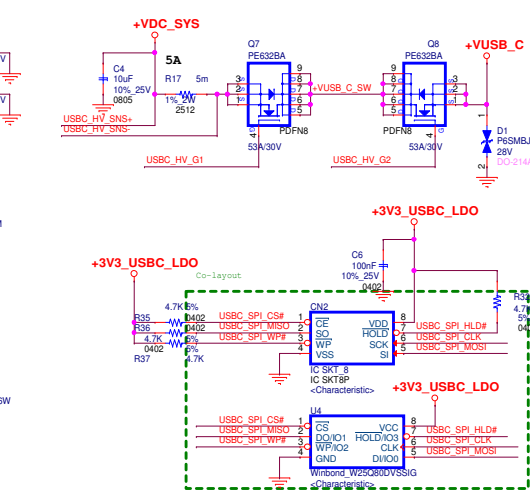
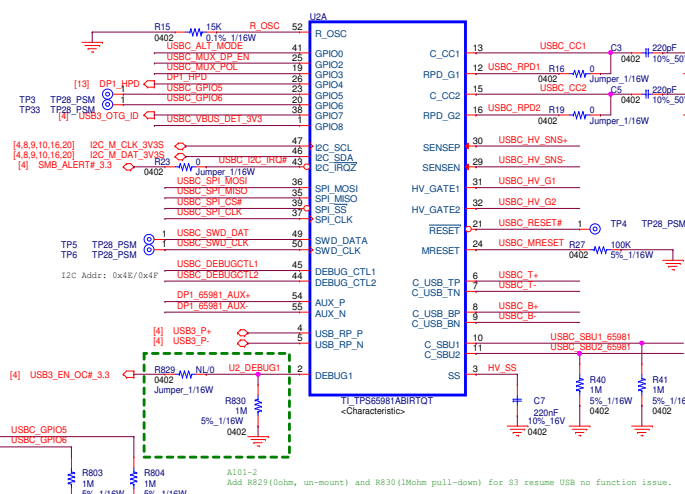
SMARC Module





For Module Board



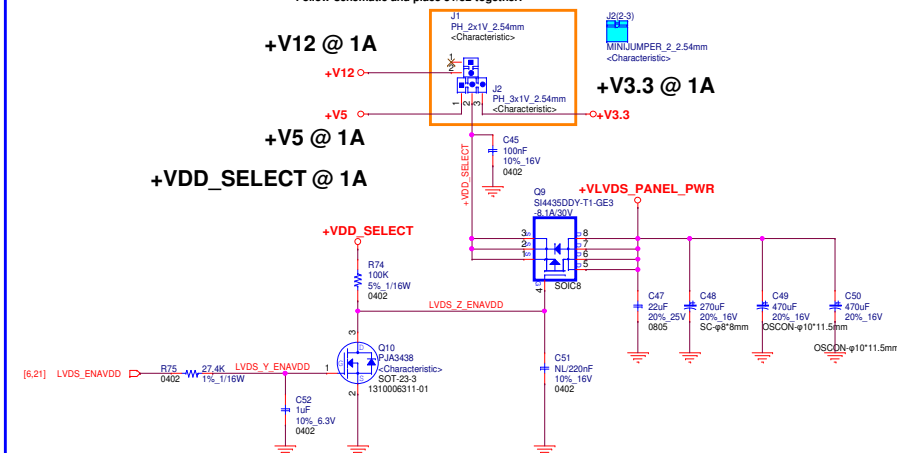


Layout Note:
ESD net 可以為了簡化修改 Net 順序

Table 1. 4-Level Control Pin Settings

LEVEL	SETTINGS
0	Option 1: Tie 1 KΩ 5% to GND. Option 2: Tie directly to GND.
R	Tie 20 KΩ 5% to GND.
F	Float (leave pin open)
1	Option 1: Tie 1 KΩ 5% to V _{CC} . Option 2: Tie directly to V _{CC} .

CAD Note :
Follow schematic and place J1/J2 together.

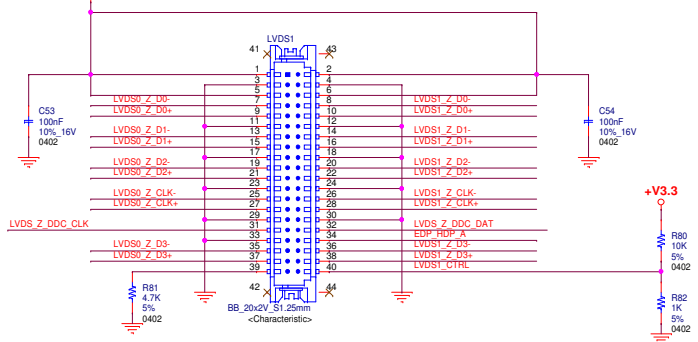
[illegible]

J4(1-2)
MINILUMPER_2_254mm
<Characteristic>

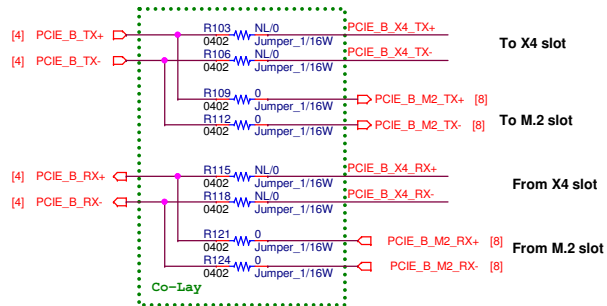
LVDS/eDP HPD select
1-2 LVDS
2-3 EDP_ HPD

J4
PH 3x1V 254mm
<Characteristic>

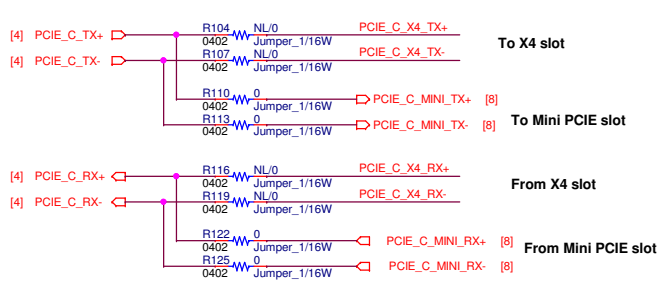
EDP_HDP_A
EDP_HDP_B [21]
EDP_HDP_C

+VLVDS_PANEL_PWR @ 1A (40mils)
+VLVDS_PANEL_PWR

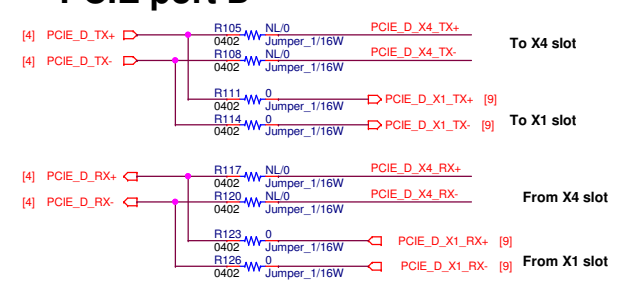
PCIE port B



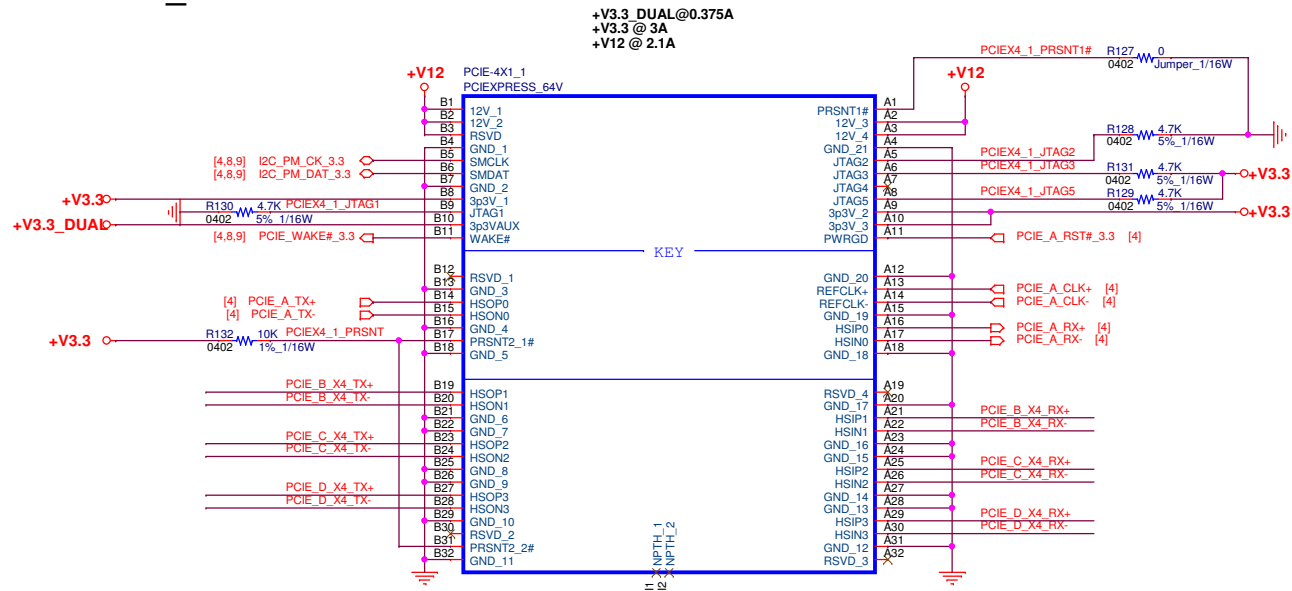
PCIE port C



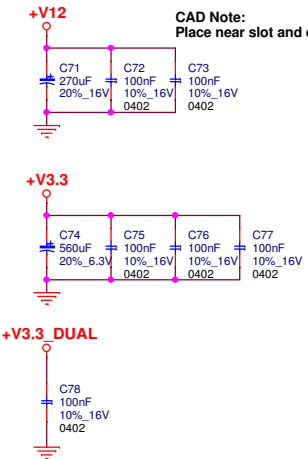
PCIE port D



PCI-E X4_Slot



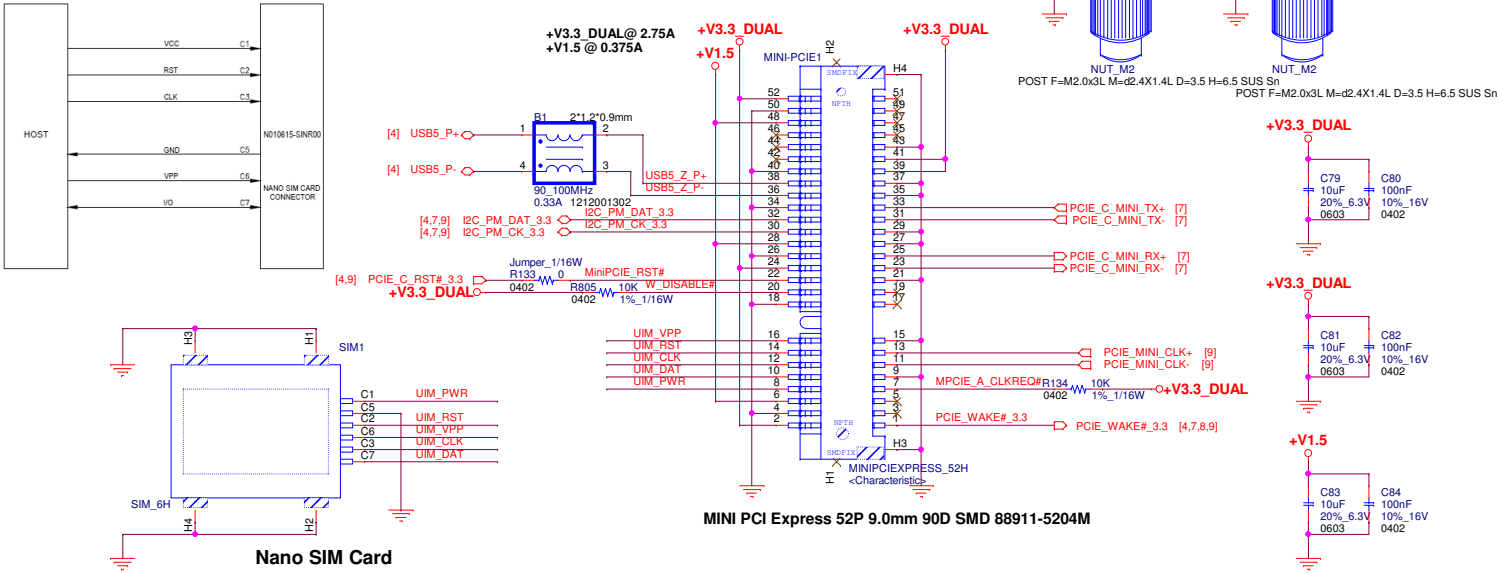
CAD Note:
Place near slot and each PWR pin.



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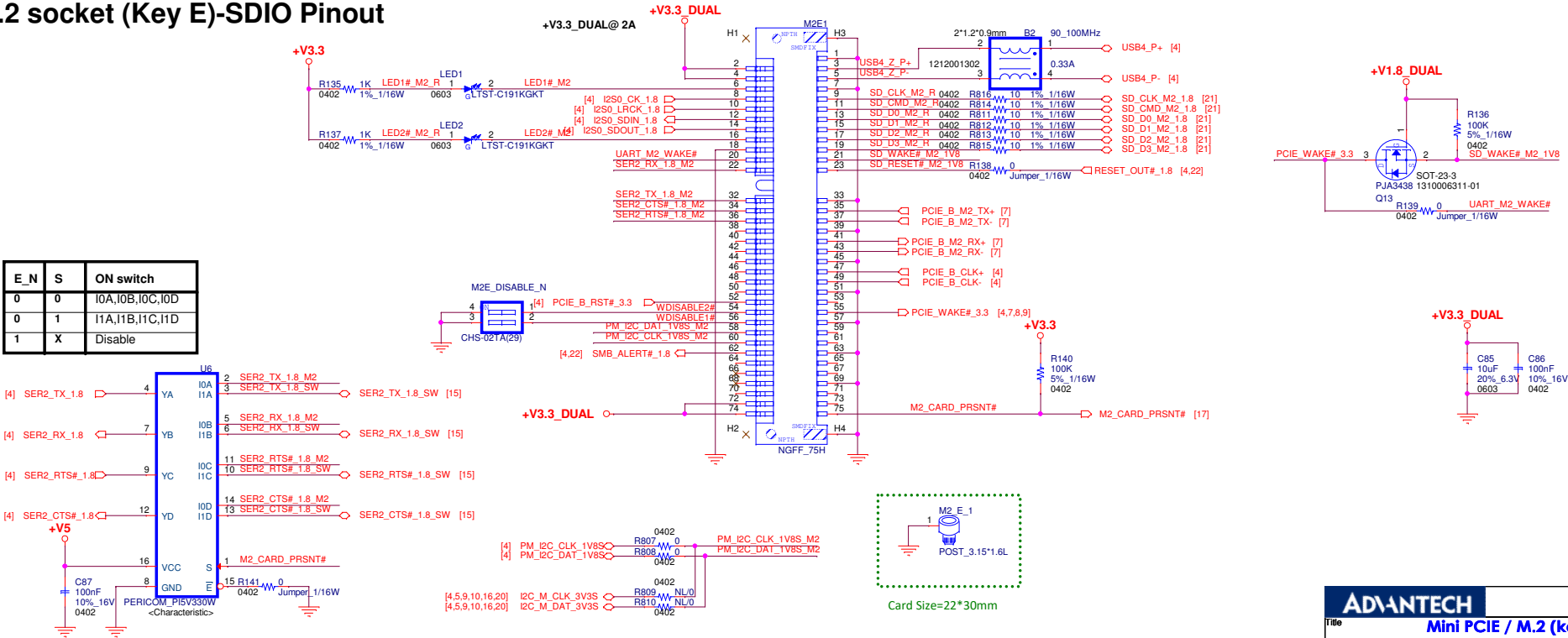
Title	PCIE X4 slot		
Size	Document Number	SOM-DB2500	Rev
Date:	Tuesday, November 19, 2019	Sheet	7 of 31

PCI Express Mini Card



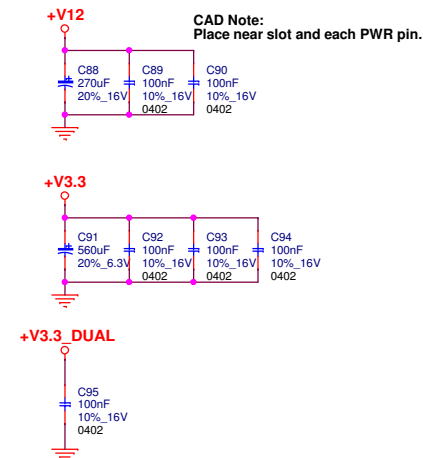
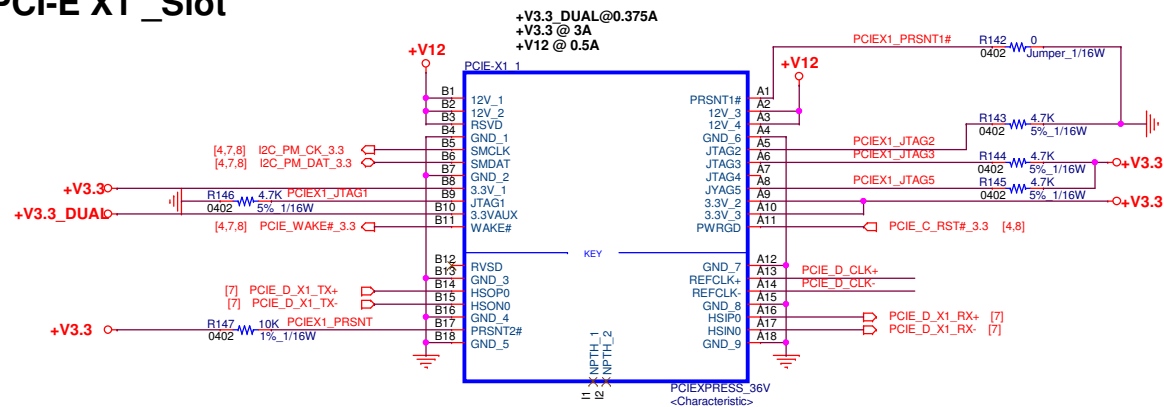
Mini PCI-E Ver 1.2			
Pin#	Name	Pin#	Name
1	WAKE#	2	3.3Vaux
3	COEX1	4	GND
5	COEX2	6	1.5V
7	CLKREQ#	8	UIM_PWR
9	GND	10	UIM_DATA
11	REFCLK-	12	UIM_CLK
13	REFCLK+	14	UIM_RESET
15	GND	16	UIM_VPP
Mechanical Key			
17	Reserved (UIM_C8)	18	GND
19	Reserved (UIM_C4)	20	W_DISABLE#
21	GND	22	PERST#
23	PERn0	24	3.3Vaux
25	PERp0	26	GND
27	GND	28	1.5V
29	GND	30	SMB_CLK
31	PETn0	32	SMB_DATA
33	PETp0	34	GND
35	GND	36	USB_D-
37	GND	38	USB_D+
39	3.3VAUX	40	GND
41	3.3VAUX	42	LED_WWAN#
43	GND	44	LED_WLAN#
45	Reserved	46	LED_WPAN#
47	Reserved	48	1.5V
49	Reserved	50	GND
51	Reserved	52	3.3VAUX

M.2 socket (Key E)-SDIO Pinout



E_N	S	ON switch
0	0	IOA,IOB,IOC,IOD
0	1	IIA,IIB,IIC,IID
1	X	Disable

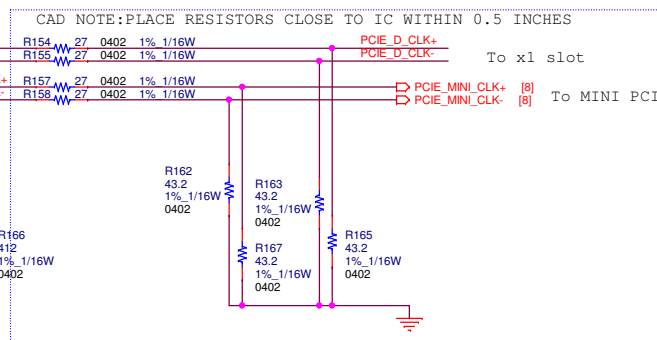
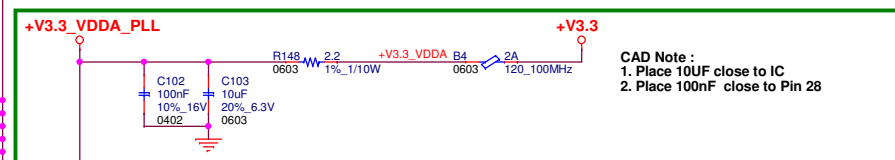
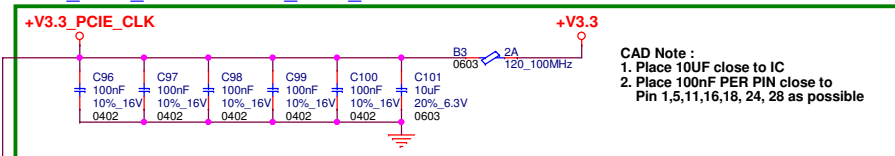
PCI-E X1 Slot



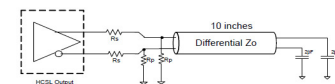
PCIE Clock Buffer

PLL (BYP#_LOBW_HIBW)	MODE
Low Mid High	Bypass PLL 100M Low BW PLL 100M Hi BW

SMB_ADR_tri	Address
Low	DA/DB
Mid	DC/DD
High	D8/D9



FAE suggestion for diff. impedance 85ohm.



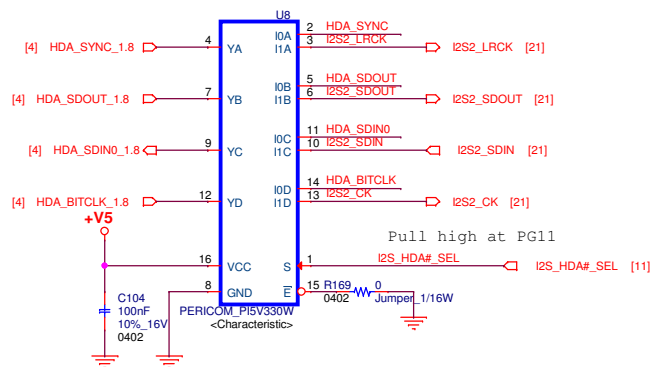
DIF Zo (Ω)	Iref (Ω)	Rs (Ω)	Rp (Ω)
100	475	33	50
85	412	27	42.2 or 43.2

ADVANTECH

Title	PCIE CLK buffer / PCIE X1 slot
-------	--------------------------------

Size	Document Number	Rev
	SOM-DB2500	A101-3
	Tuesday, November 19, 2019	

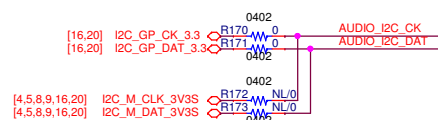
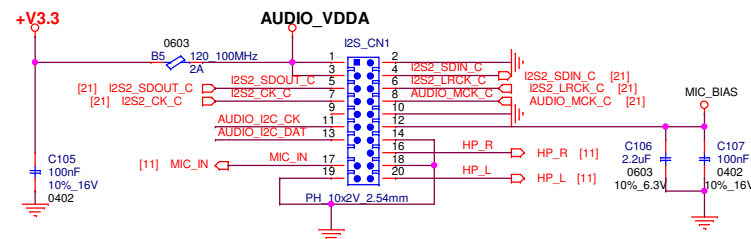
Date: Tuesday, November 19, 2019 Sheet 9 of 31



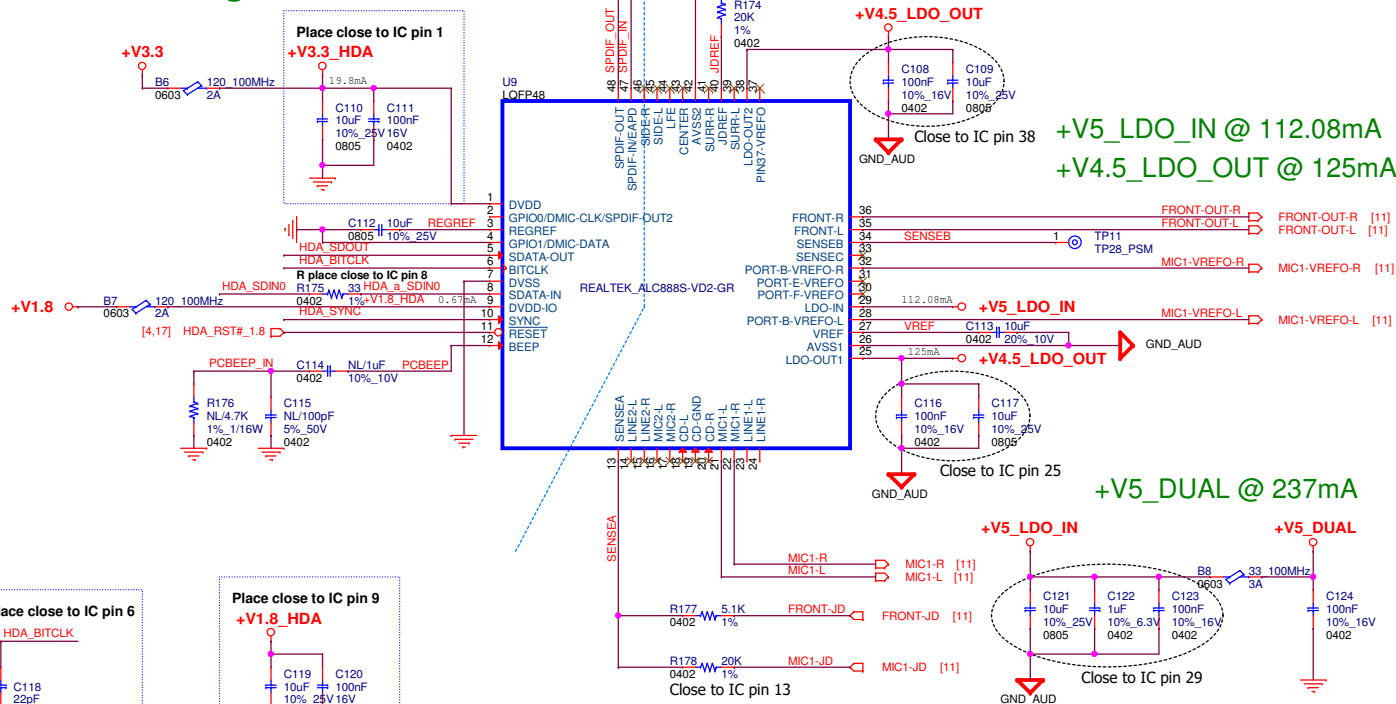
E_N	S	ON switch
0	0	IOA,IOB,IOC,IOD
0	1	IIA,IIB,IIC,IID
1	X	Disable

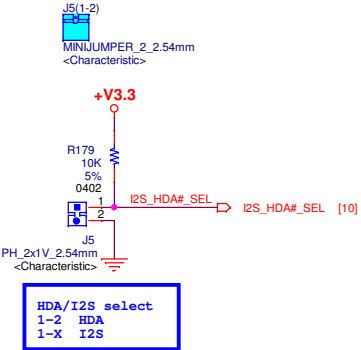
Digital GND Audio GND

I2S2 connect to CODEC
(SOM-EA52 with TI_TLV320AIC3107IRSBR, Address:0x18)

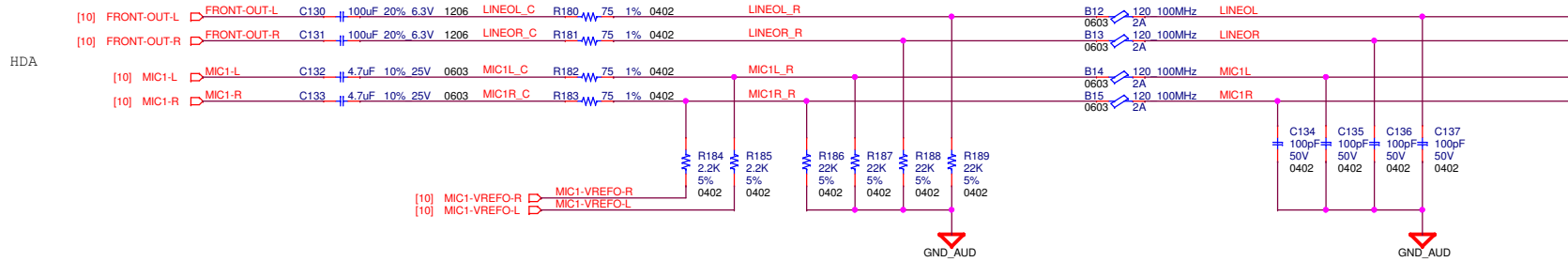
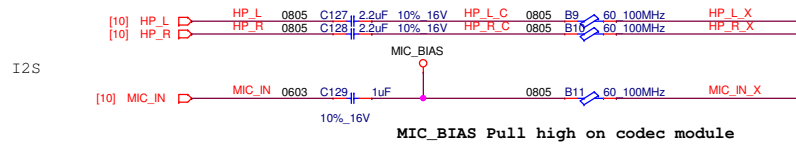
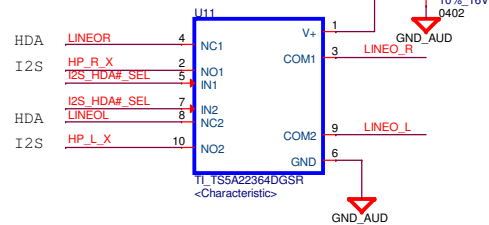
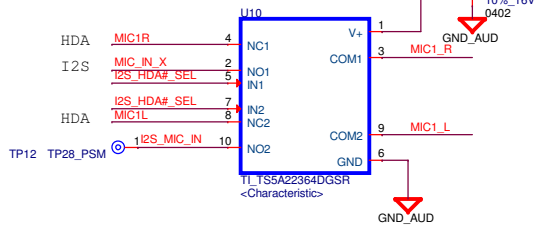


+V3.3 @ DVDD=19.8mA
+V1.8 @ DVDDIO=0.67mA

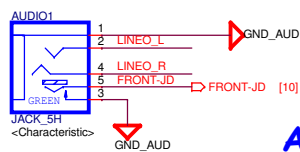




IN	FUNCTION TABLE
0	NC TO COM,COM TO NC
1	NO TO COM,COM TO NO

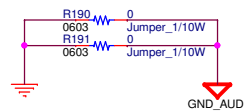
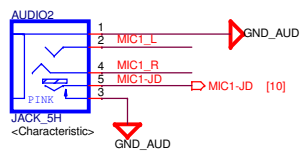


LINE OUT

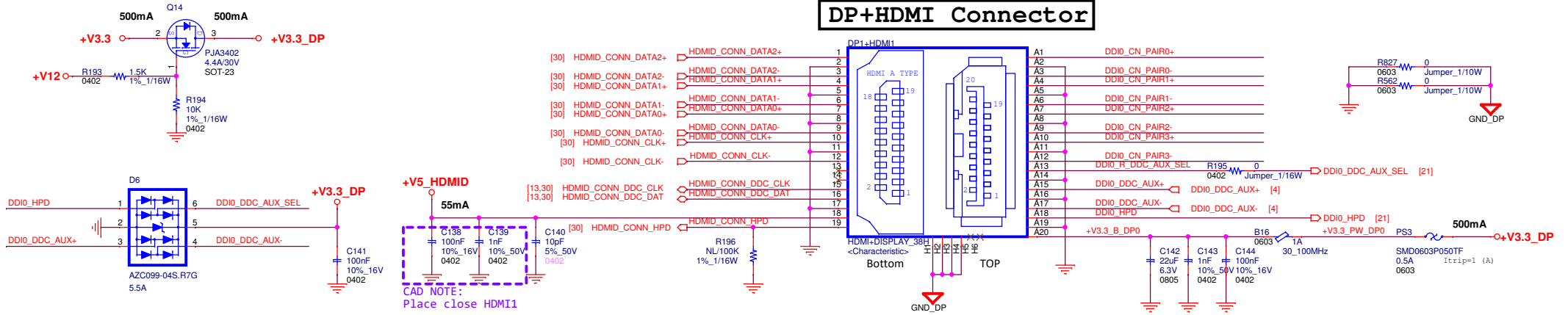


AUDIO Jack

MIC IN

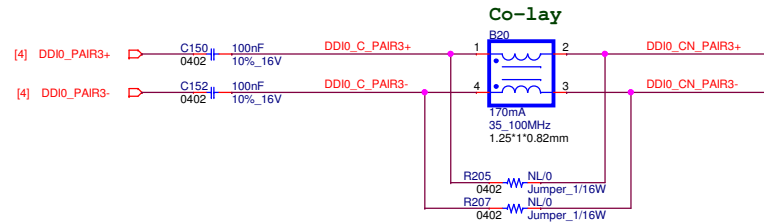
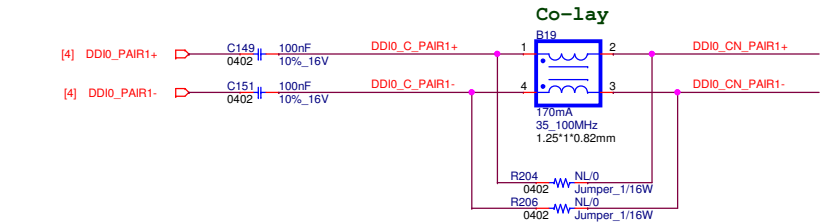
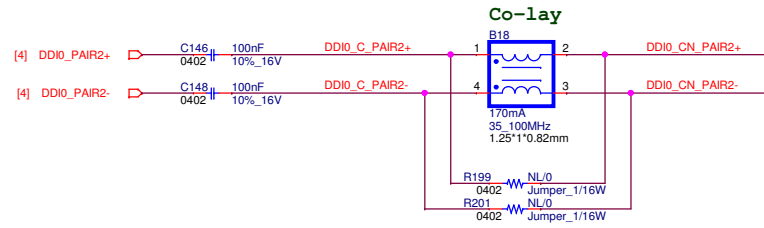
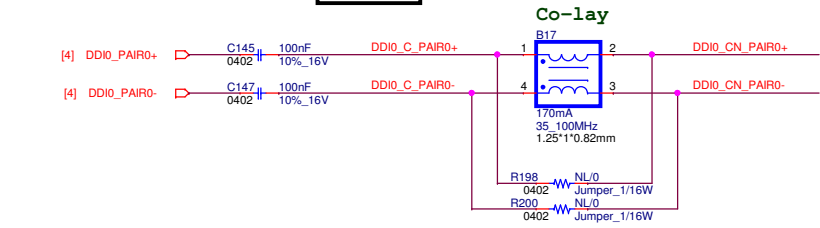


DPO

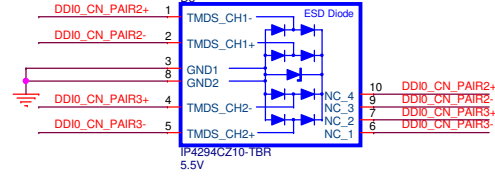
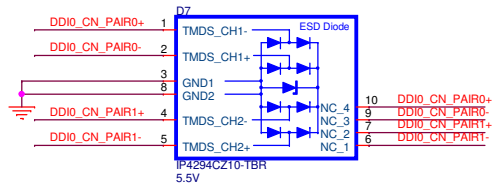


Pin A13 : Config 1
 High : HDMI device detect
 Low : DP device detect
 Operating Temperature: -25~85 degree

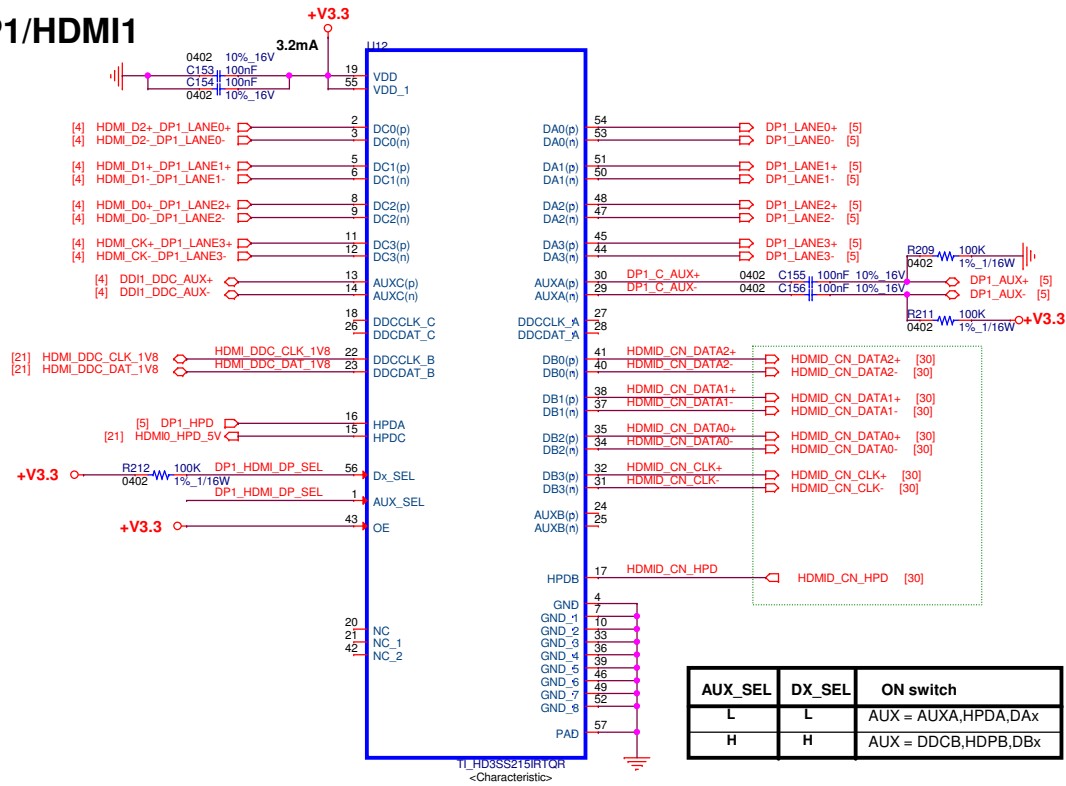
Bead CAD Note: Bead place them close to connector



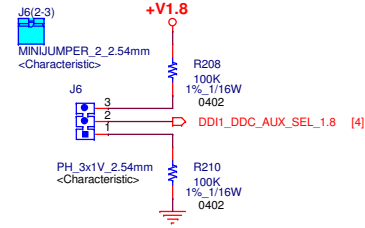
CAD Note: ESD Diode place them close to connector



DP1/HDMI1



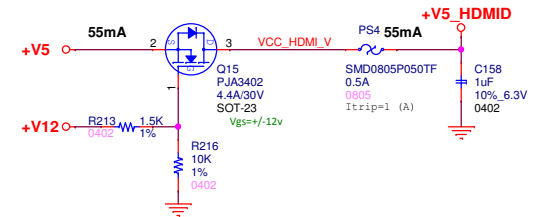
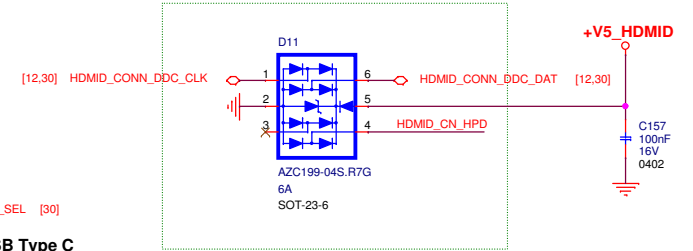
only for modules supporting
DP++ at HDMI/DP1
1-2 AUX
2-3 DDC



```
DP1/HDMI1 select
1-2 DP @ USB Typ
2-3 HDMI CONN
```

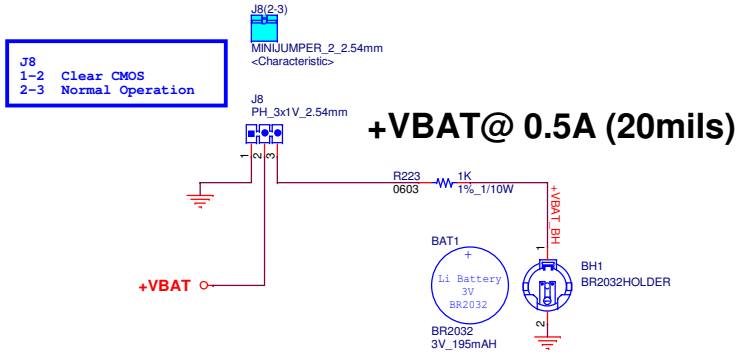
1-2 DP @ USB Type C
2-3 HDMI CONN

L :DP @ USB Type C
H :HDMI CONN

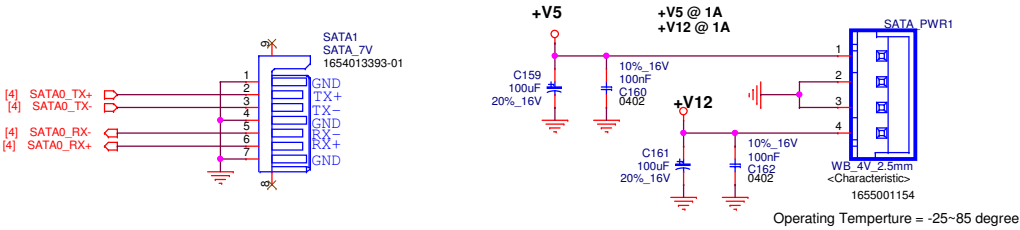


AUX_SEL	DX_SEL	ON switch
L	L	AUX = AUXA,HPDA,DAx
H	H	AUX = DDCB,HDPB,DBx

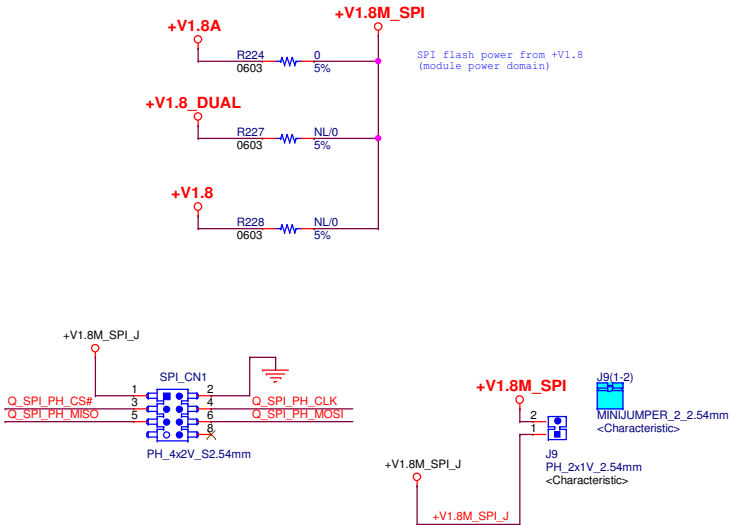
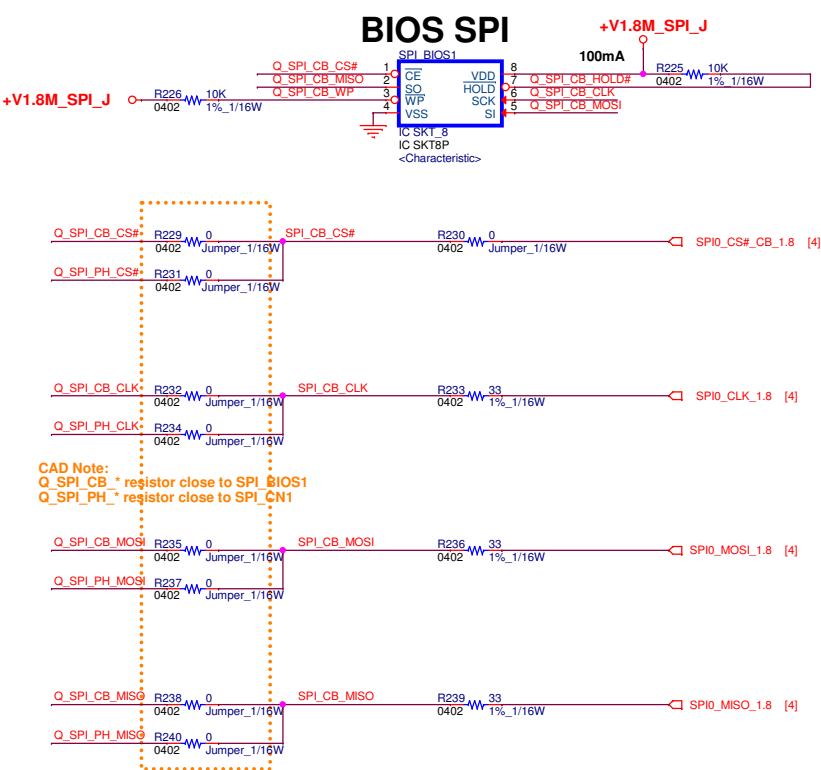
RTC BATTERY



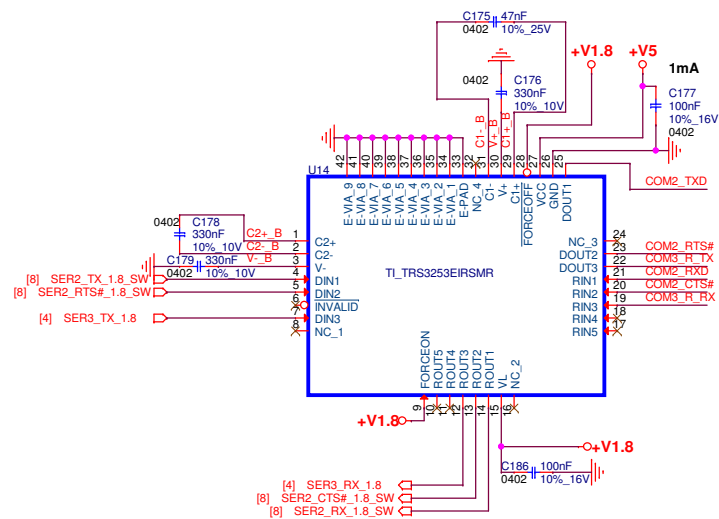
SATA



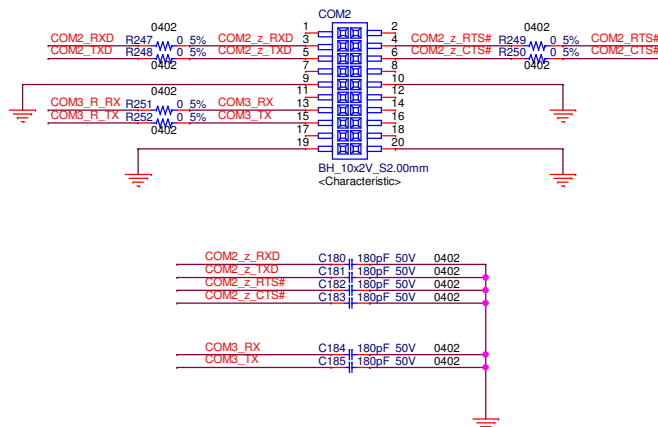
SPI



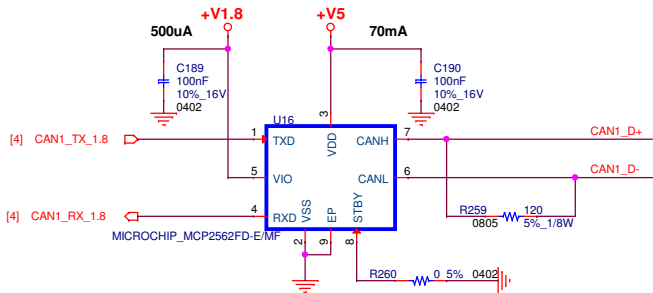
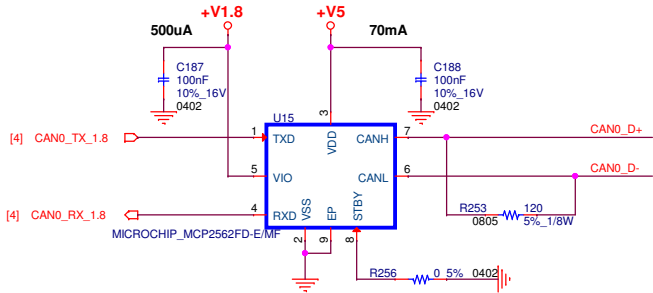
COM2/3:RS232



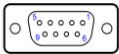
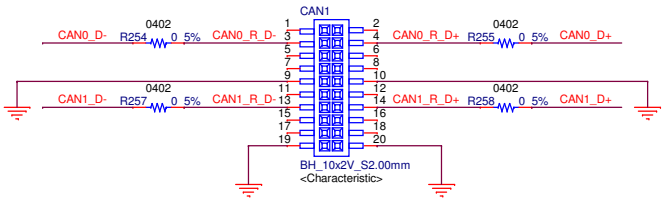
COM2/3 BOX HEADER



CAN Transceiver



CAN BOX HEADER



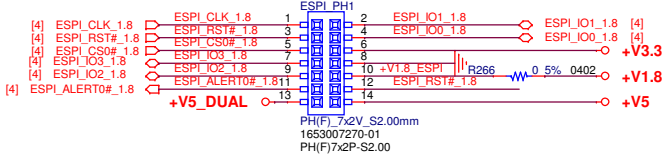
DE-9

9 Pin (male) D-Sub CAN Bus PinOut

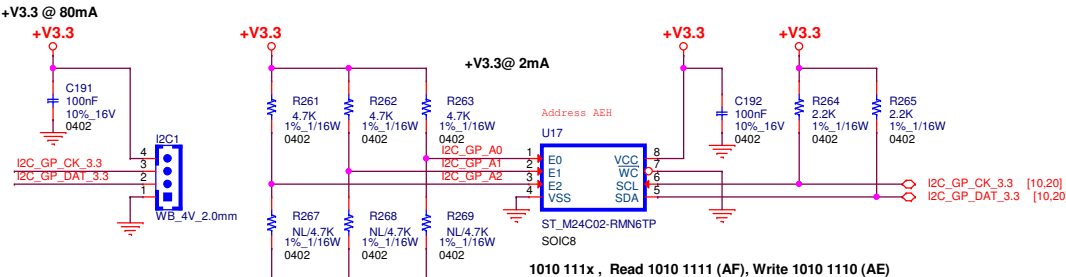
Pin #	Signal names	Signal Description
1	Reserved	Upgrade Path
2	CAN_L	Dominant Low
3	CAN_GND	Ground
4	Reserved	Upgrade Path
5	CAN_SHLD	Shield, Optional
6	GND	Ground, Optional
7	CAN_H	Dominant High
8	Reserved	Upgrade Path
9	CAN_V+	Power, Optional

eSPI Pin Header

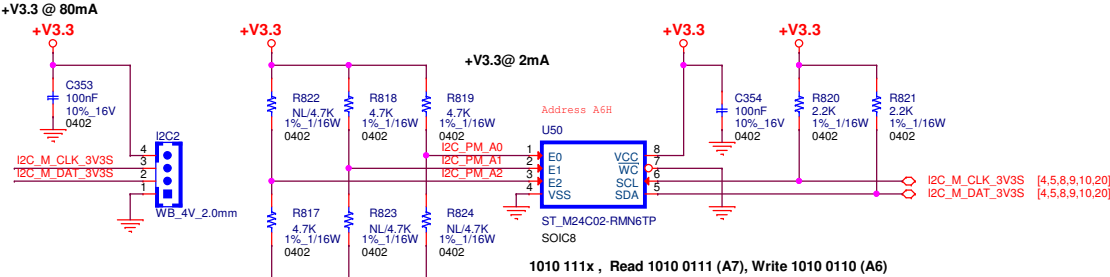
LPC CLK / eSPI_CLK
LAD_0 / eSPI_IO_0
LAD_1 / eSPI_IO_1
LAD_2 / eSPI_IO_2
LAD_3 / eSPI_IO_3
LFRAME# / eSPI_CS
SERIRQ / eSPI_ALERT
LRESET# / eSPI_RESET#



I2C GP



I2C PM



Device type identifier ⁽¹⁾				Chip Enable address			RW
b7	b6	b5	b4	b3	b2	b1	b0
1	0	1	0	E2	E1	E0	RW

1. The most significant bit, b7, is sent first.

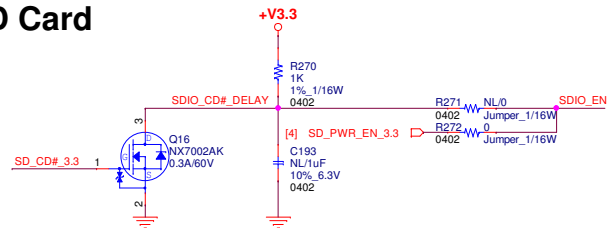
ADVANTECH

Title CAN BUS/eSPI/I2C

Size Document Number SOM-DB2500 Rev A101-3

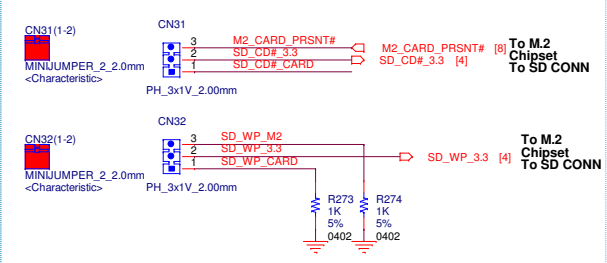
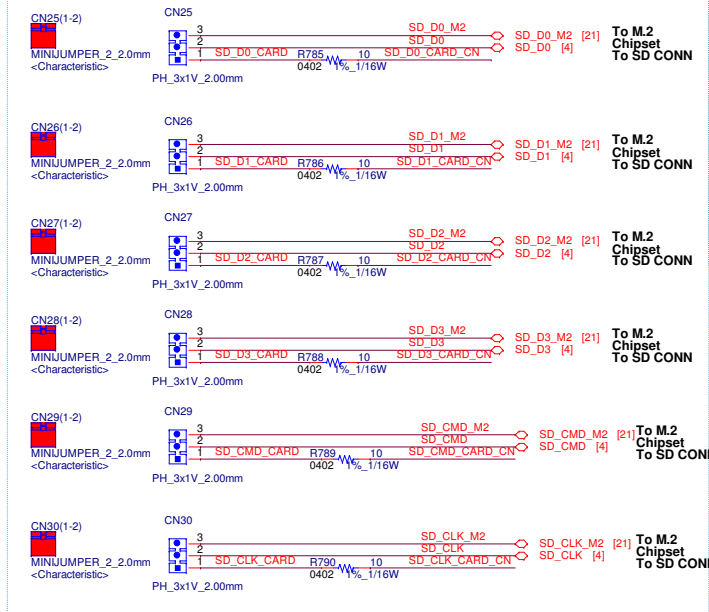
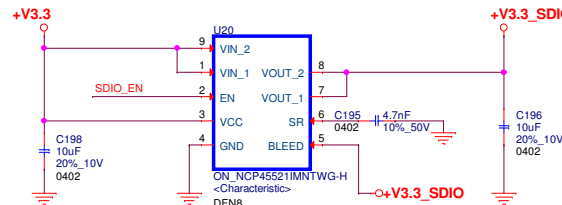
Date: Tuesday, November 19, 2019 Sheet 16 of 31

SD Card



+V3.3

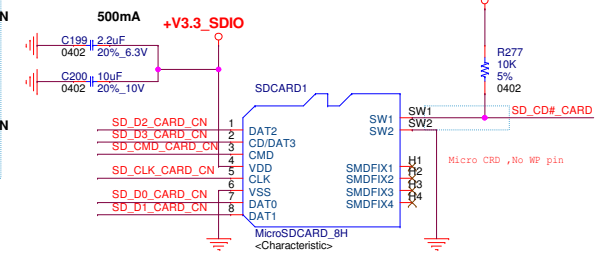
+V3.3_SDIO @ 0.5A



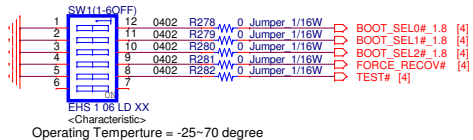
SD to SD CARD CONN or M.2

Micro SD Card

MicroSD Card Socket:
No Card SW1 --open-- SW2
Card Inserted SW1 --close-- SW2

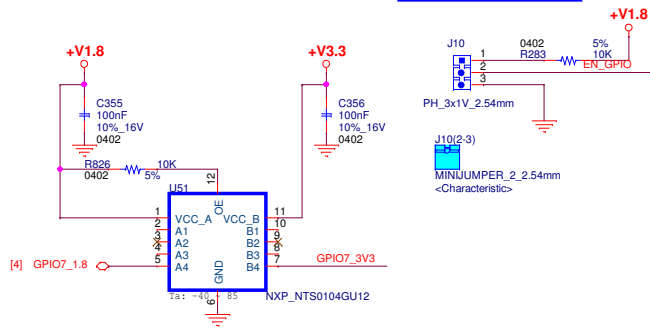
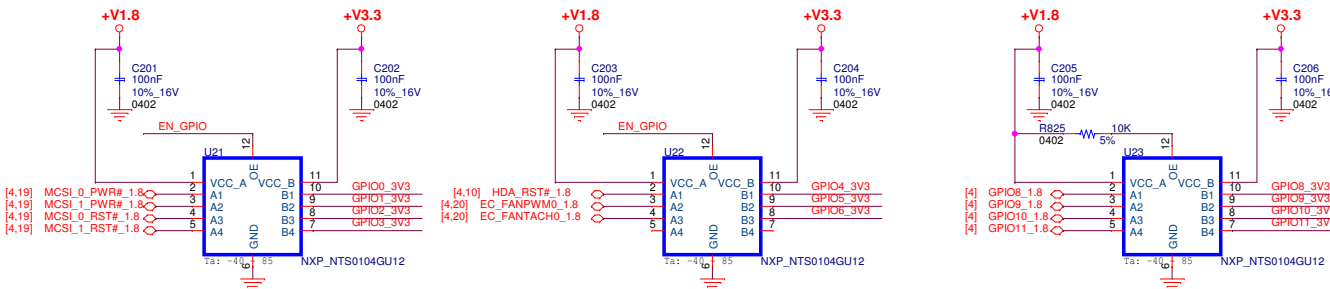


BOOT SELECT



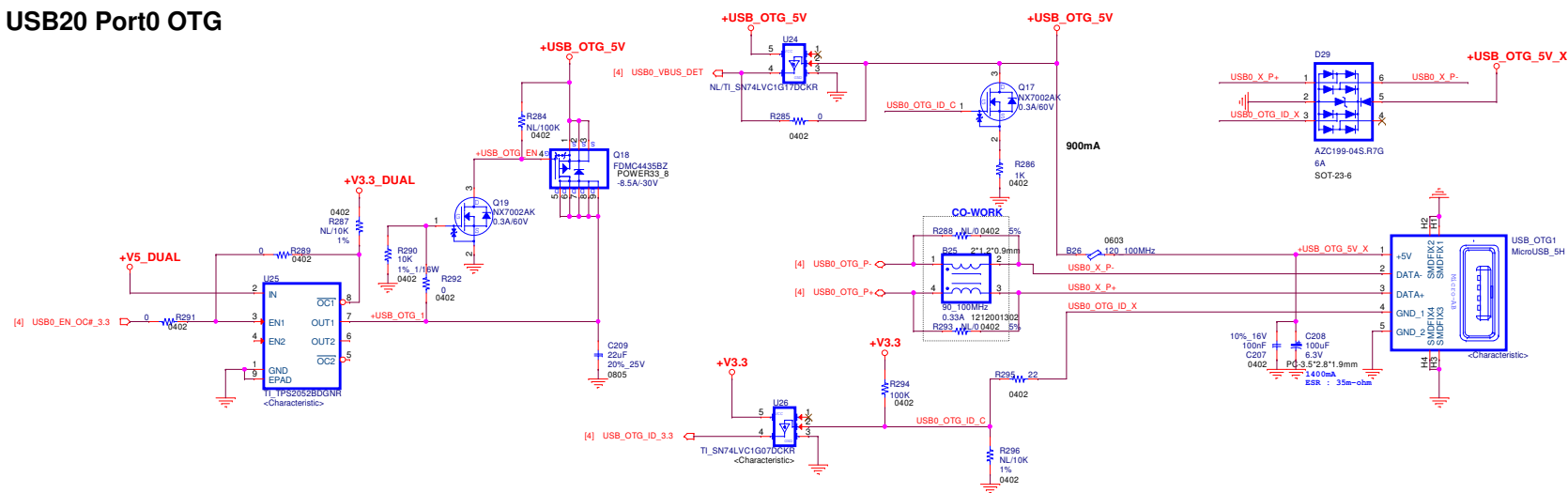
	Carrier Connection			Boot Source
	BOOT_SEL2#	BOOT_SEL1#	BOOT_SEL0#	
0	GND	GND	GND	Carrier SATA
1	GND	GND	Float	Carrier SD Card
2	GND	Float	GND	Carrier eSPI (CS0#)
3	GND	Float	Float	Carrier SPI (CS0#)
4	Float	GND	GND	Module device (NAND, NOR) – vendor specific
5	Float	GND	Float	Remote boot (GBE, serial) – vendor specific
6	Float	Float	GND	Module eMMC Flash
7	Float	Float	Float	Module SPI

GPIO Pin Header

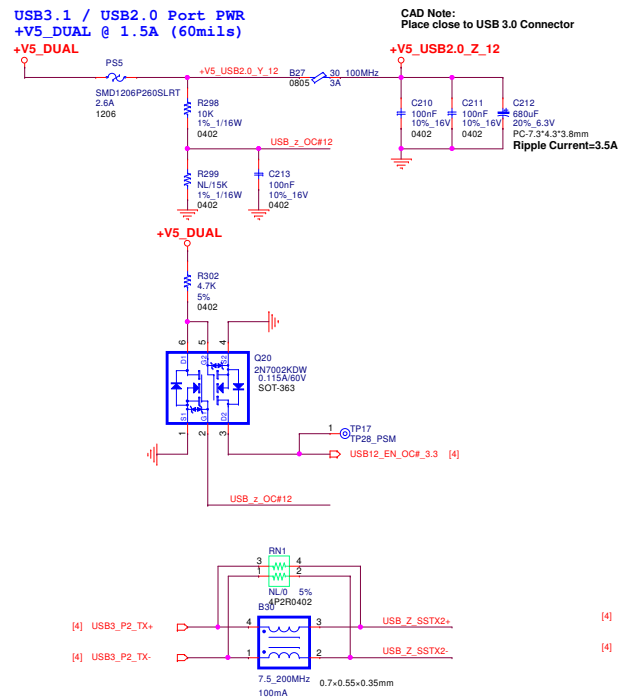


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SDCARD/Boot SEL/GPIO			
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USB20 Port0 OTG



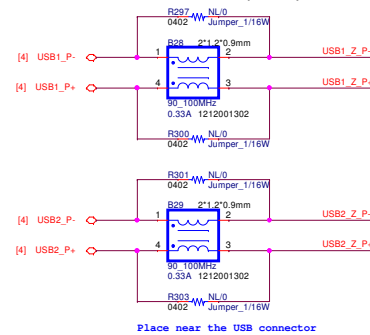
USB20 Port1/2 & USB30 Port2



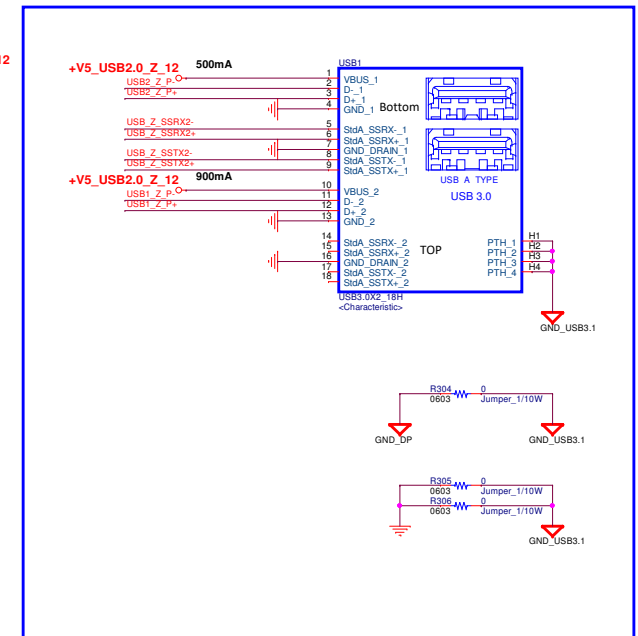
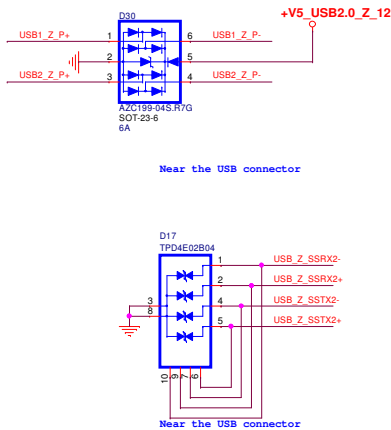
Layout Note 1:
Bead net 可以為

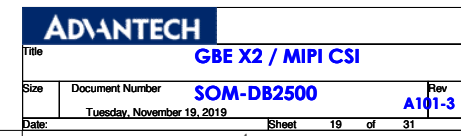
Layout Note 2:
Each pair co-layout bead overlap resistor.

Layout Note:
ESD net 可以為了順線修改 Net 順序

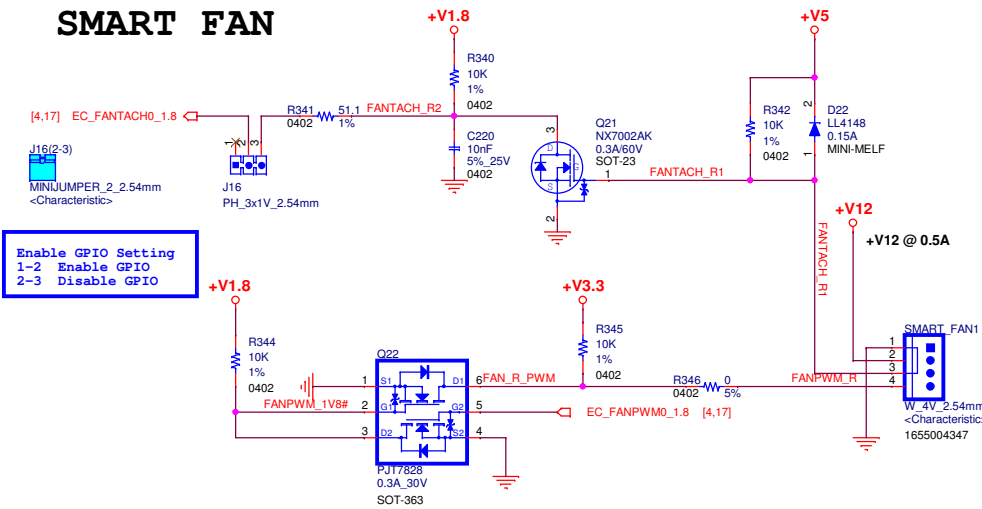


Near the USB connector

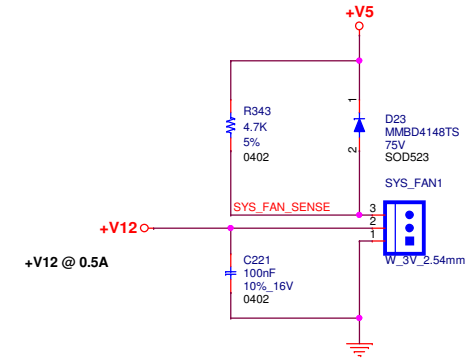




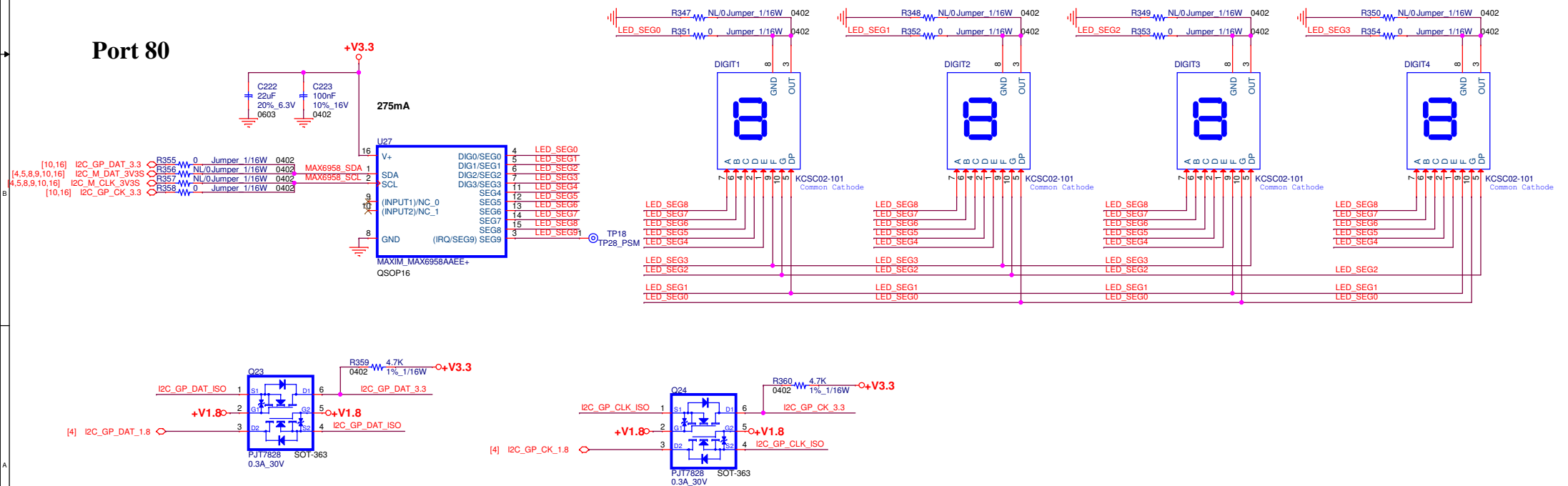
SMART FAN



SYSTEM FAN



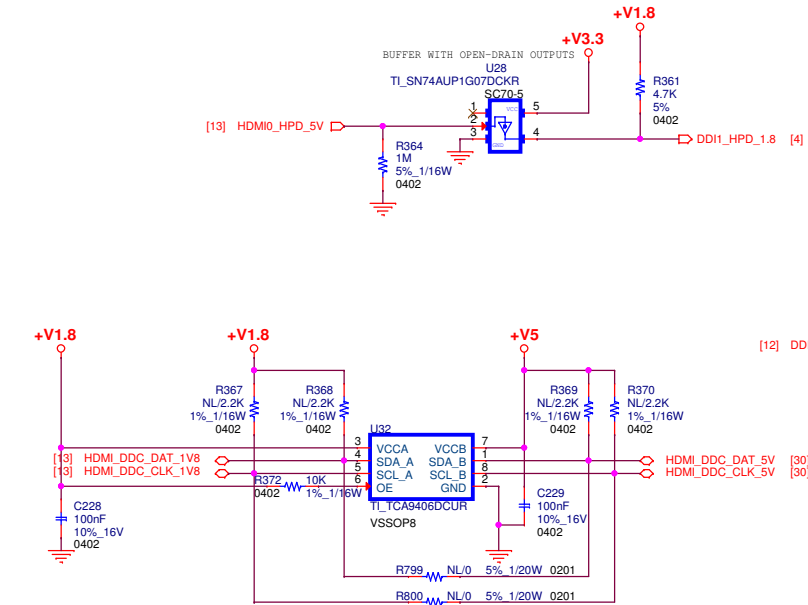
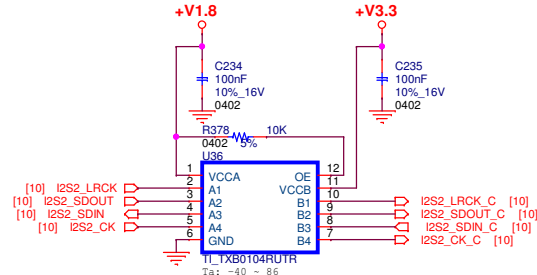
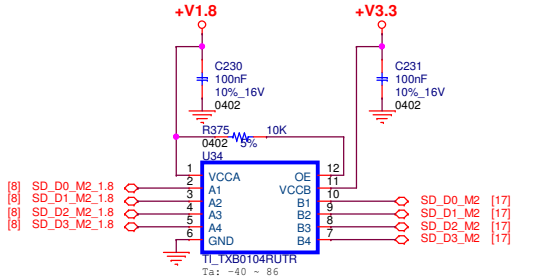
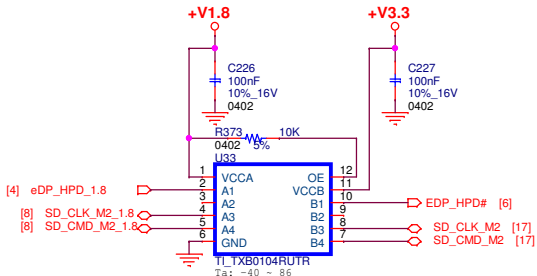
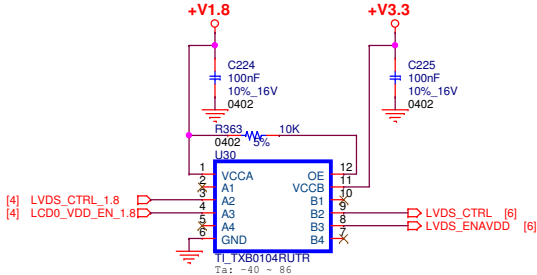
Port 80



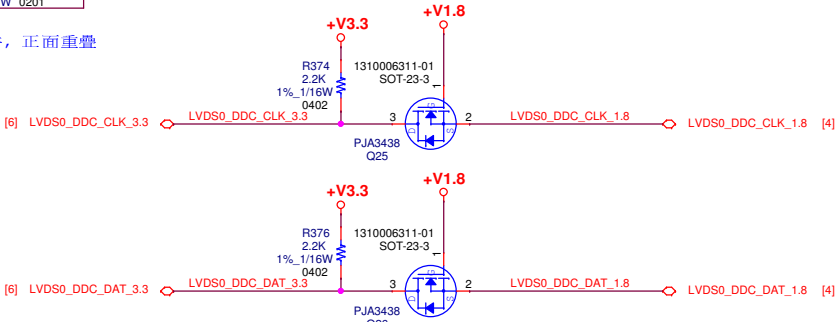
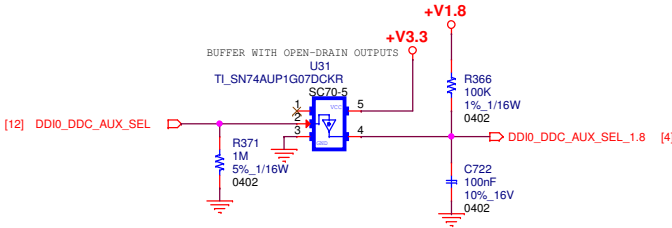
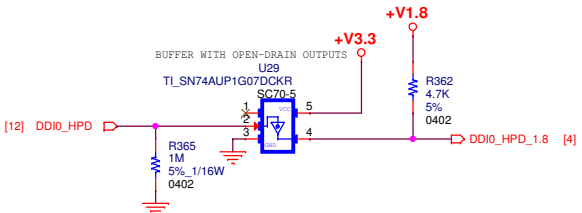
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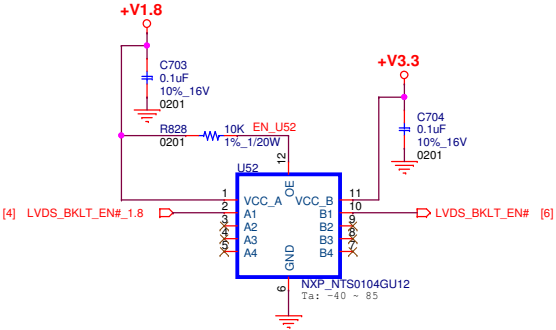
Push-Pull Level shifter



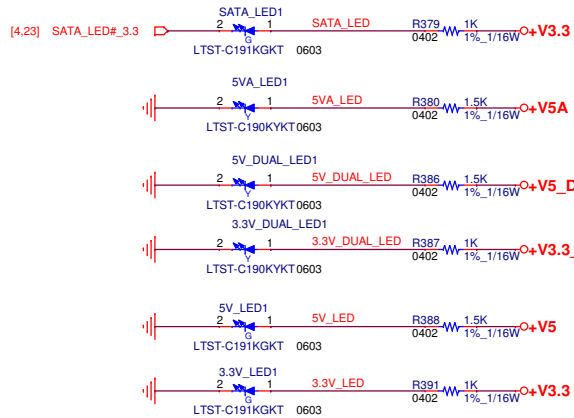
U32與R799/R800 Co-layout 單一上件，正面重疊



Open-Drain Level shifter



LED



SATA LED

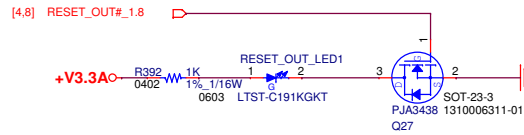
+V5A LED

+V5_DUAL LED

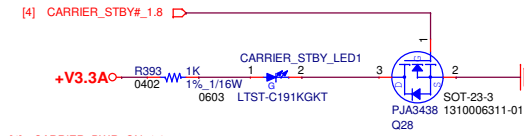
+V3.3_DUAL LED

+V5 LED

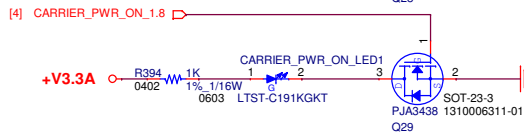
+V3.3 LED



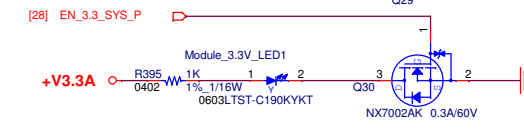
RESET_OUT#_1.8 LED



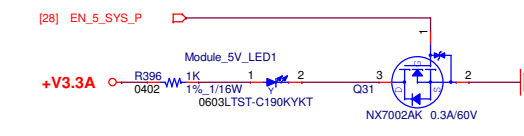
CARRIER_STBY# LED



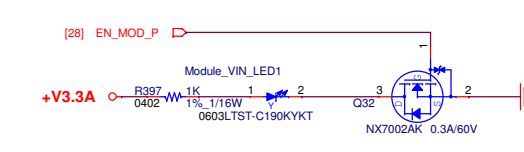
CARRIER_PWR_ON LED



Module 3.3V LED

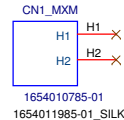
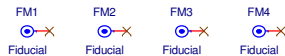


Module 5V LED

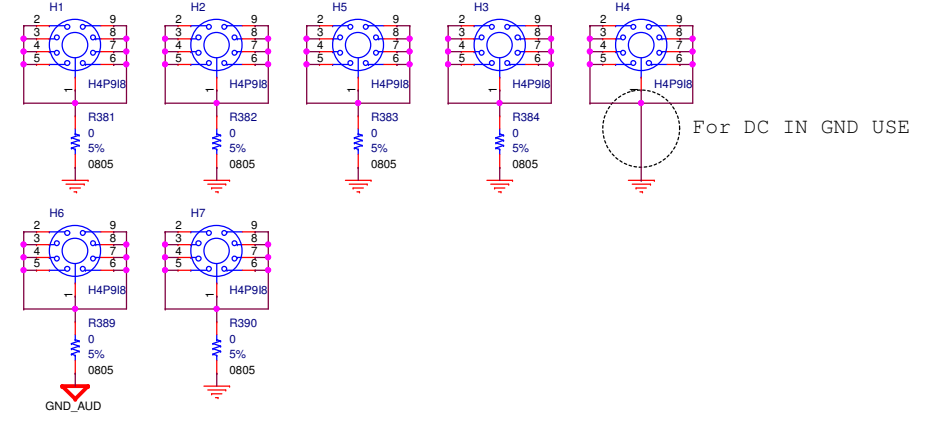


Module +V_MOD_IN LED

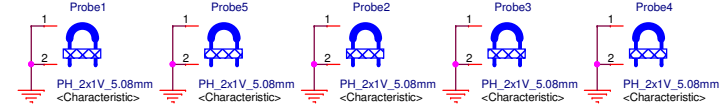
FM/PCB



SCREW HOLE

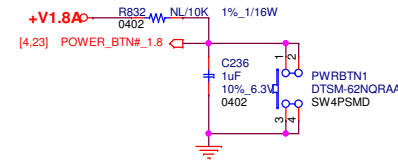


PROBE

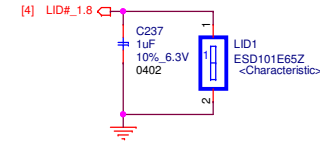


Button / Pin Header / Switch

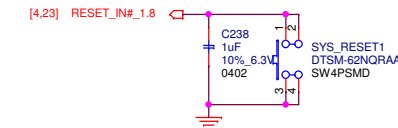
Power button



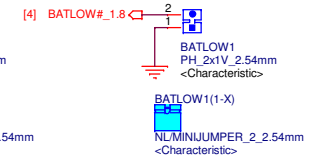
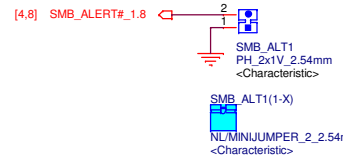
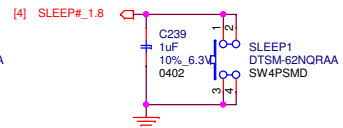
LID Switch



Reset button



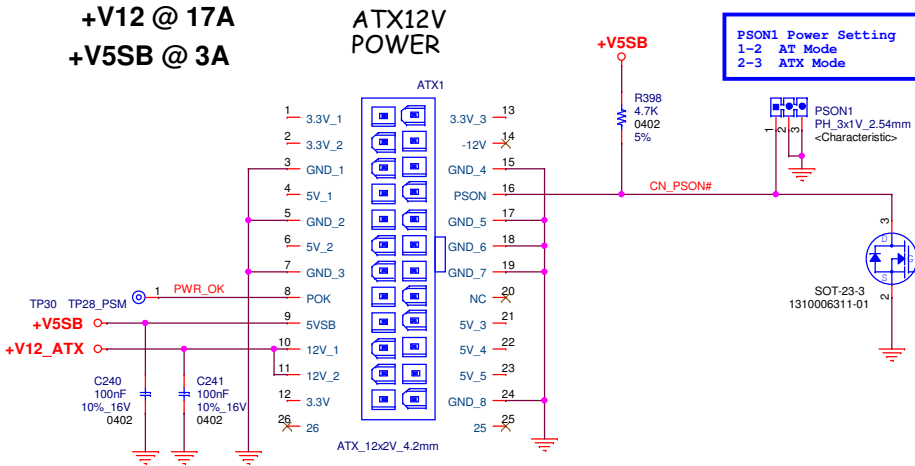
Sleep button



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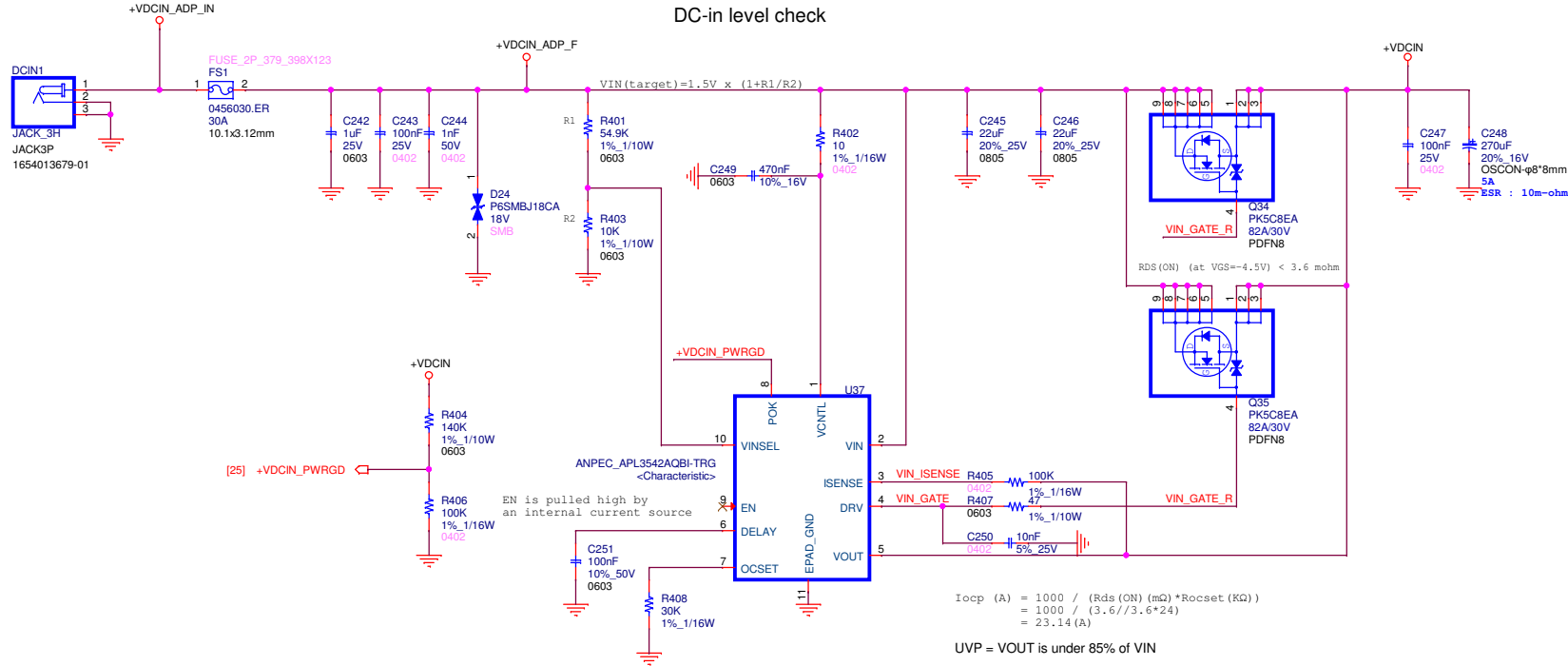
+V12 @ 17A
+V5SB @ 3A

**ATX12V
POWER**



DC-in level check

**DC-IN
(12v)**



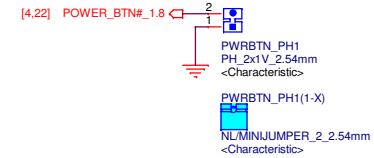
$$I_{ocp} (A) = 1000 / (R_{ds(ON)} (m\Omega) * R_{ocset} (K\Omega))$$

$$= 1000 / (3.6 / 3.6 * 24)$$

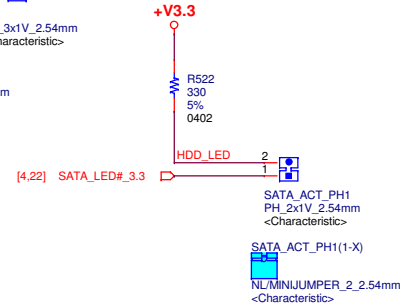
$$= 23.14 (A)$$

UVP = VOUT is under 85% of VIN

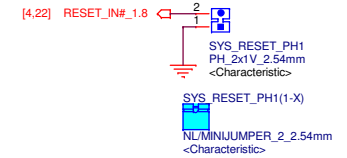
PWRBTN Pin Header



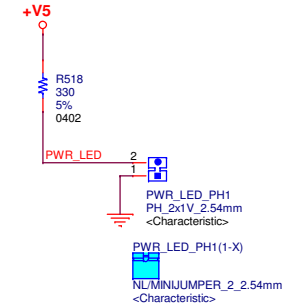
SATA ACT# Pin Header



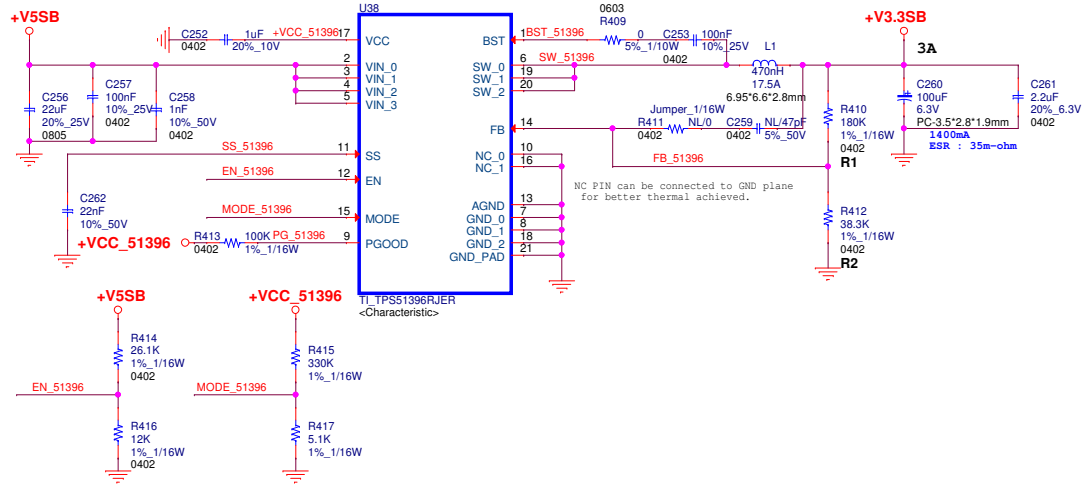
SYS RESET Pin Header



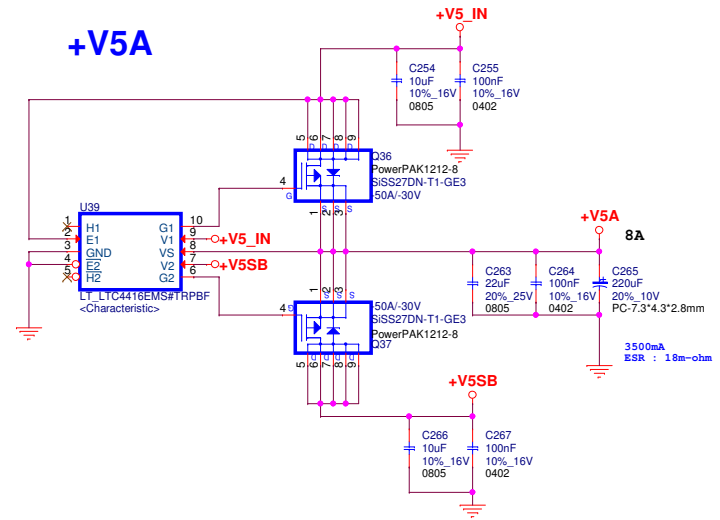
Power LED Pin Header



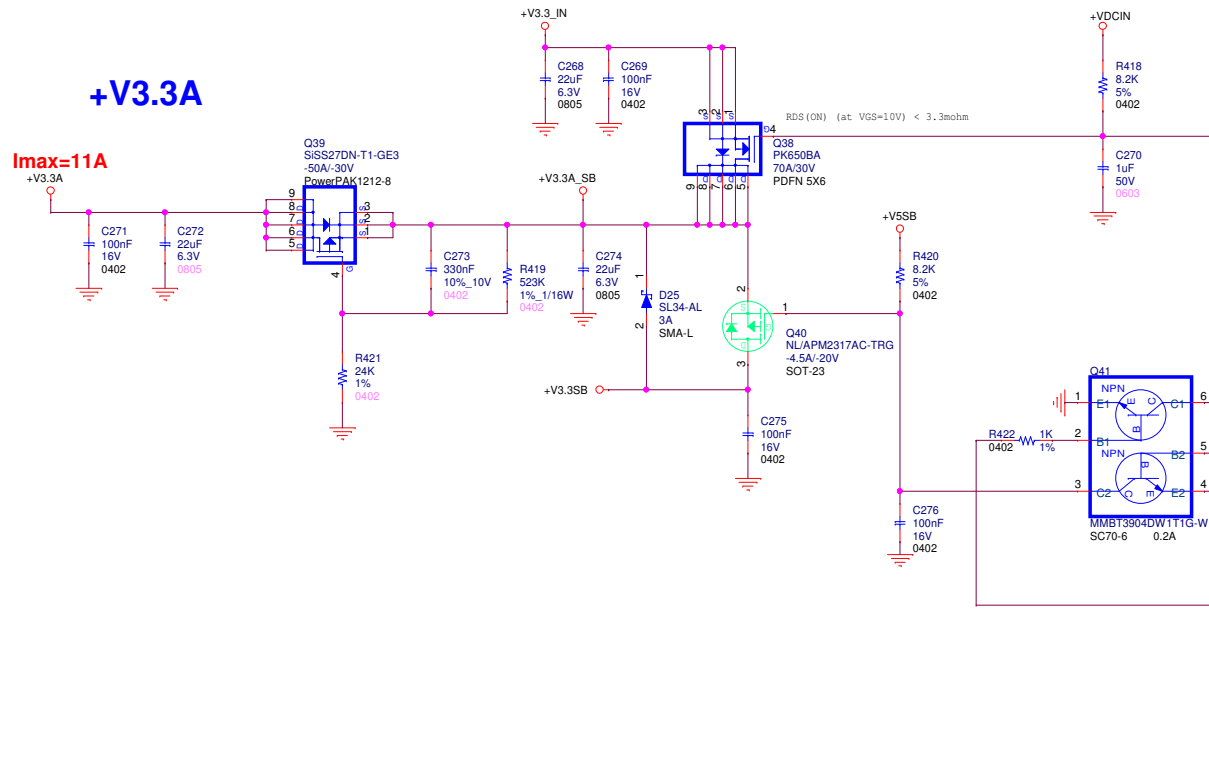
+V3.3SB



+V5A



+V3.3A

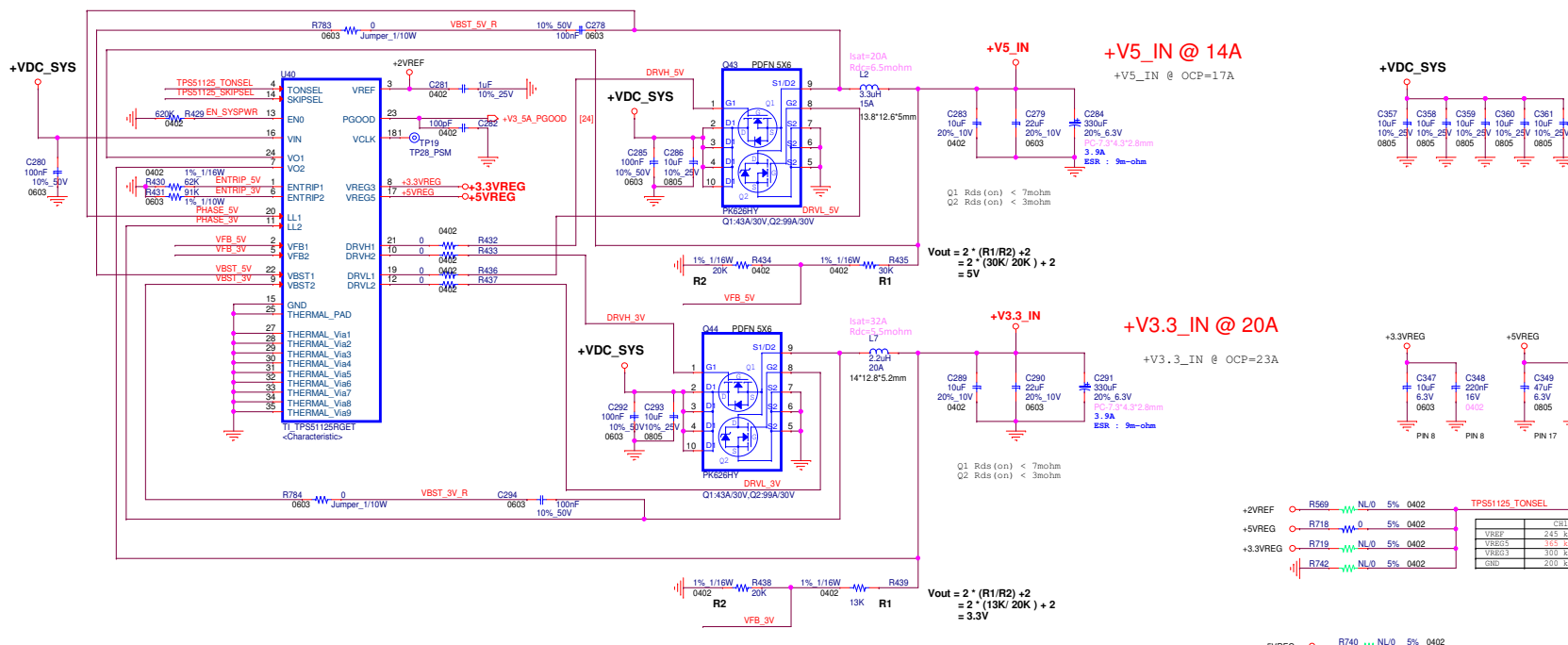


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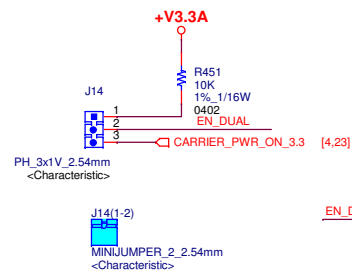
Title: +V5A/+V3.3A

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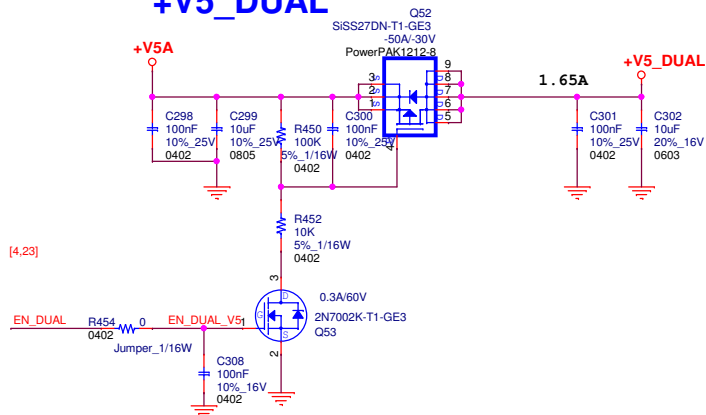
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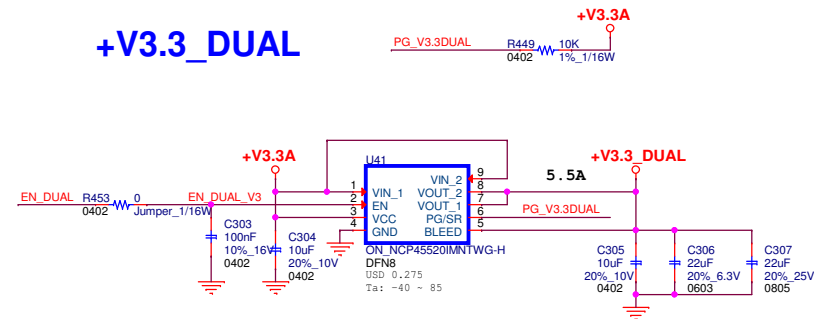
Standby Voltage control
1-2 Always Enabled
2-3 Control by CARRIER_PWR_ON



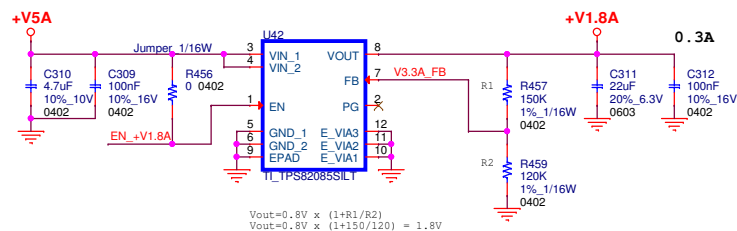
+V5_DUAL



+V3.3_DUAL



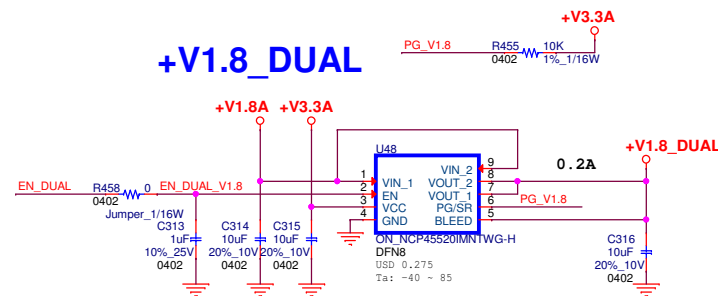
+V1.8A



$$V_{out} = 0.8V \times (1 + R1/R2)$$

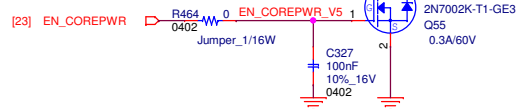
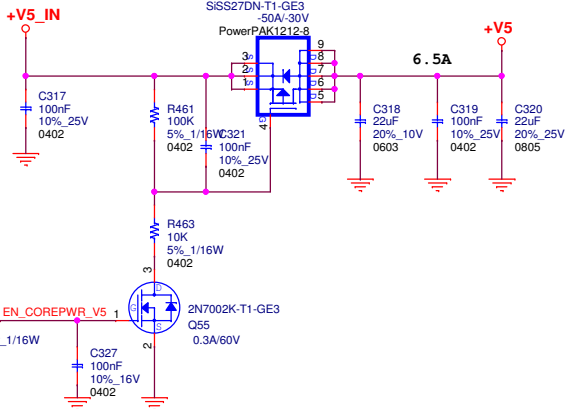
$$V_{out} = 0.8V \times (1 + 150/120) = 1.8V$$

+V1.8_DUAL

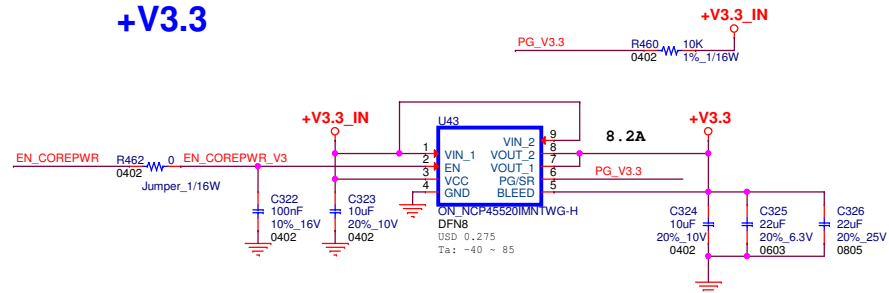


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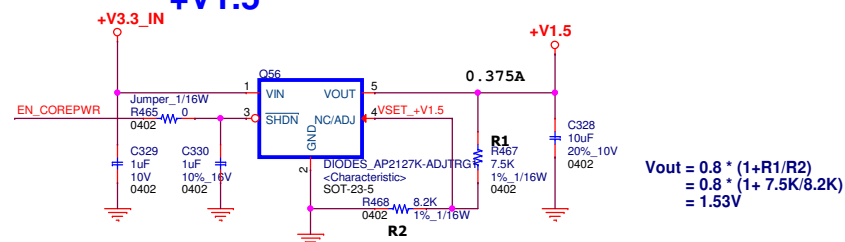
+V5



+V3.3

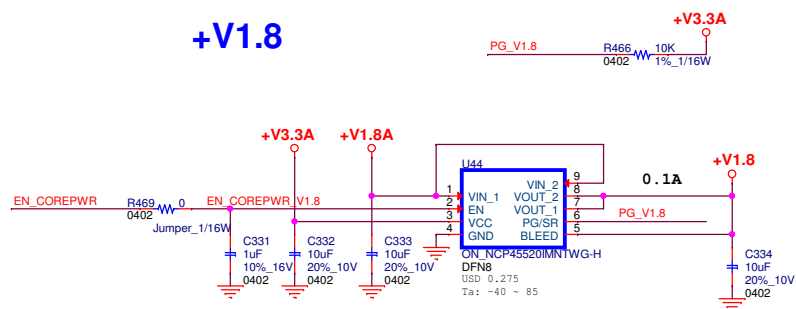


+V1.5

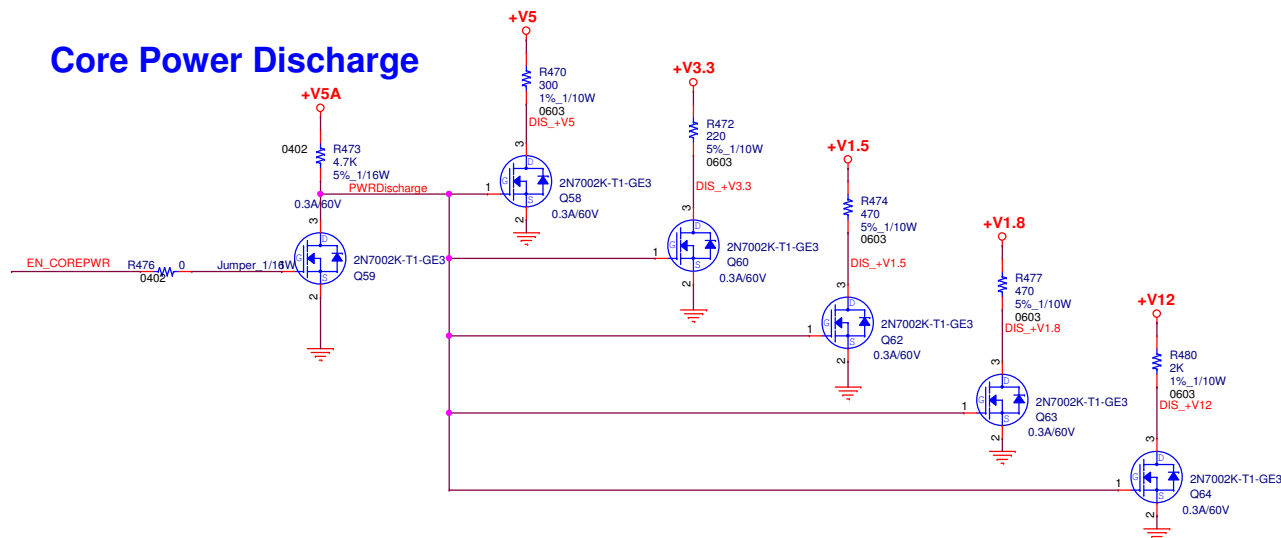


$$V_{out} = 0.8 * (1 + R1/R2) = 0.8 * (1 + 7.5K/8.2K) = 1.53V$$

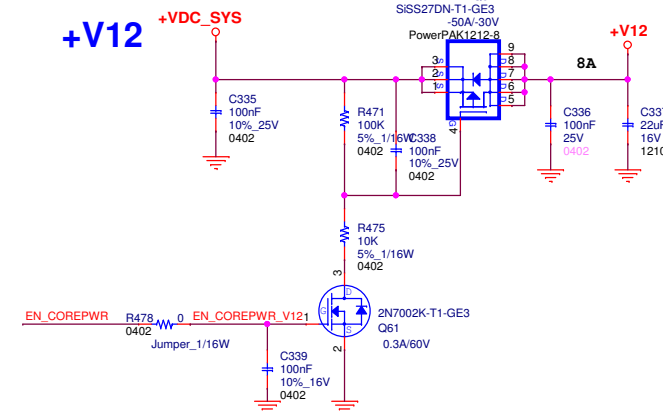
+V1.8



Core Power Discharge

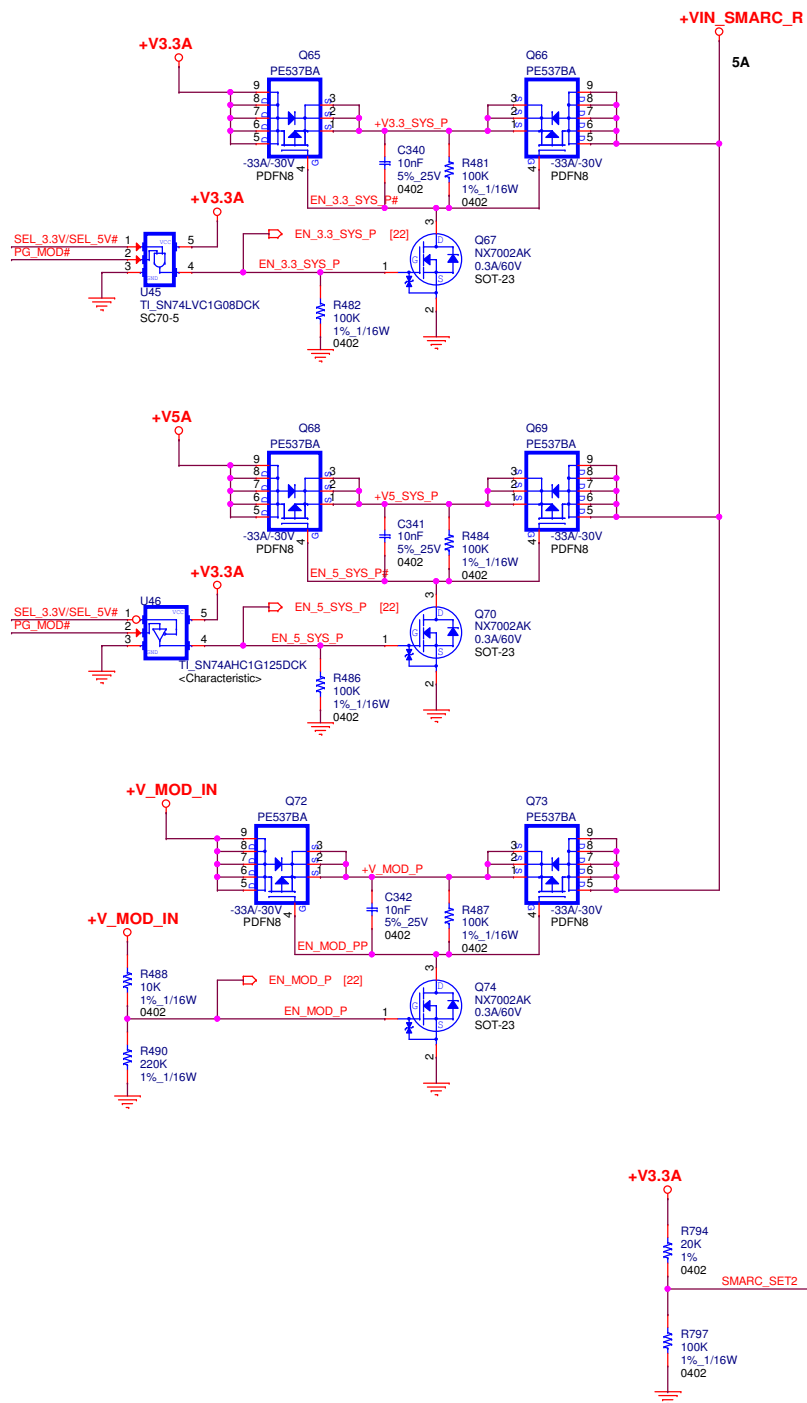


+V12

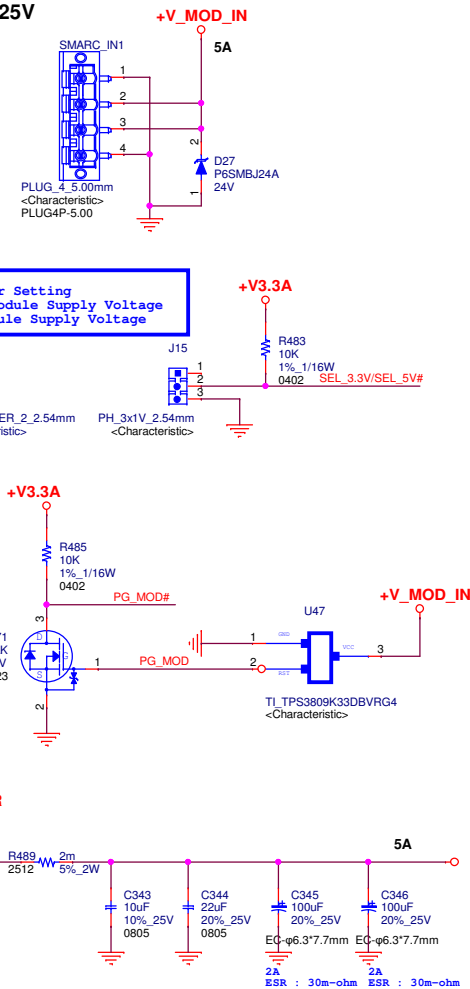


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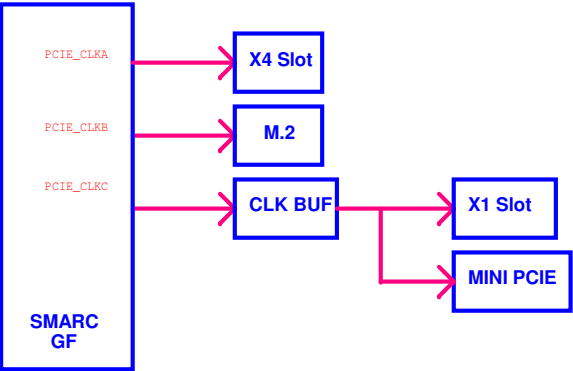


+V_MOD_IN=3V~5.25V



Module Power Setting
 1-2 3.3V Module Supply Voltage
 2-3 5V Module Supply Voltage

PCIE Clock



I2C

