MIOe-DB5000 A101-3

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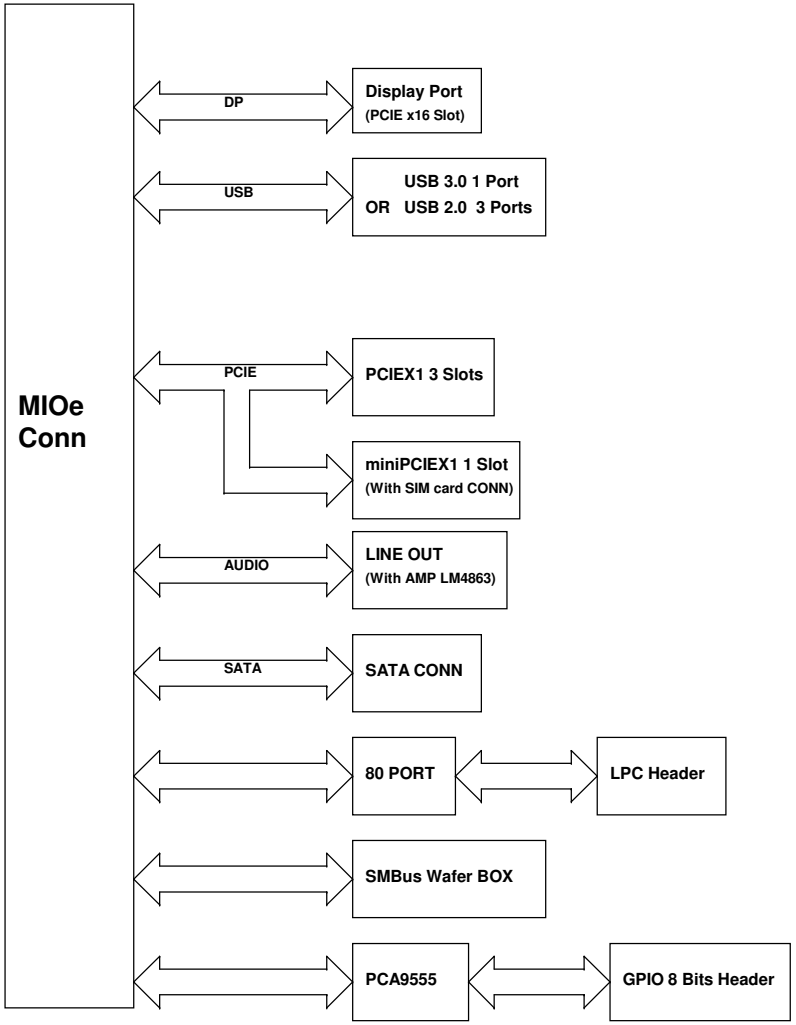
Board Diagram



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Title	Block Diagram	
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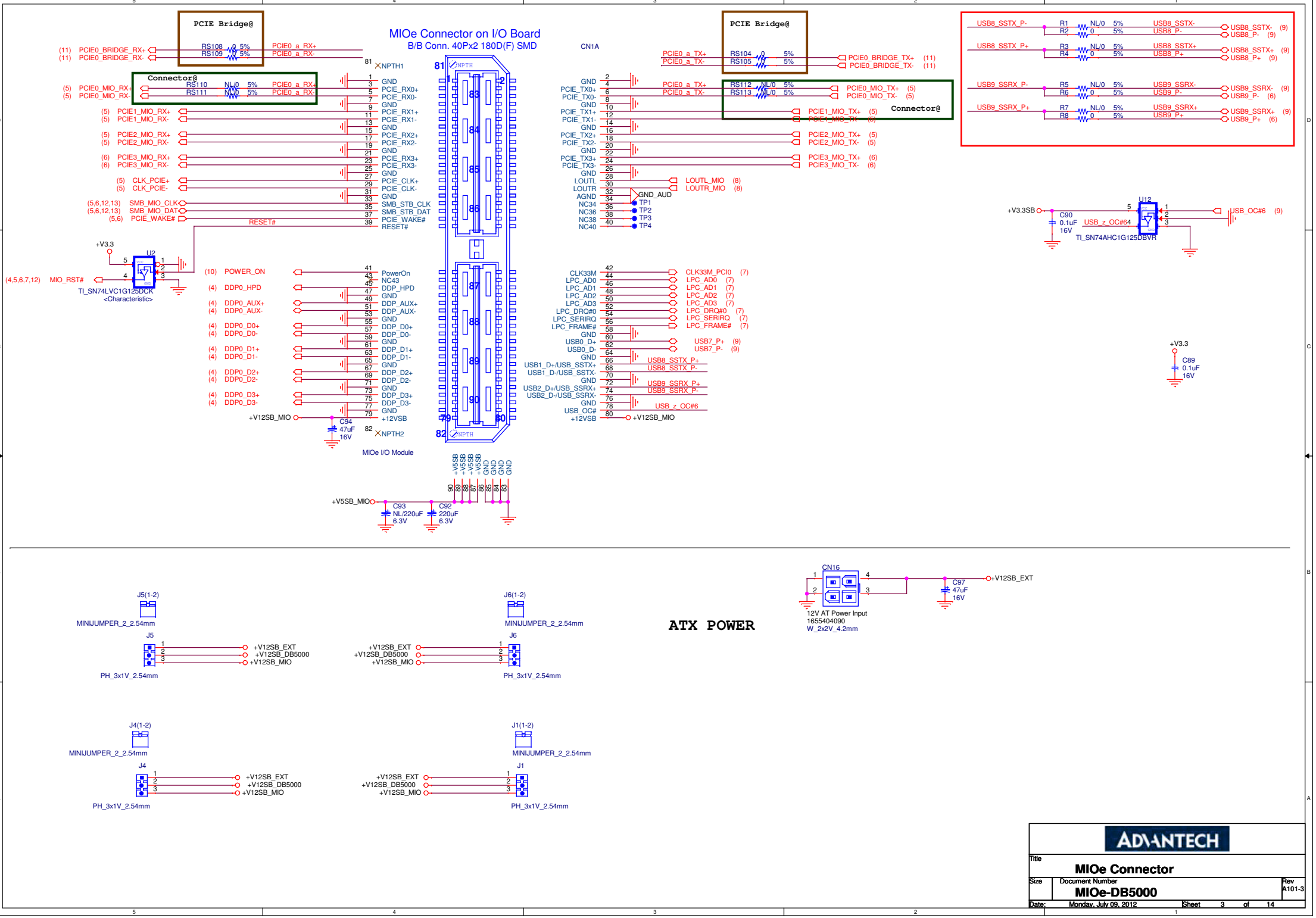
MIOe Connector on I/O Board
B/B Conn. 40Px2 180D(F) SMD
PCIE Bridge@
Connector@
MIOe I/O Module
CN1A
ATX POWER
J5(1-2)
MINIJUMPER_2_2.54mm
J5
PH_3x1V_2.54mm
J6(1-2)
J6
J4(1-2)
J4
J1(1-2)
J1
CN16
12V AT Power Input
1655404090
W_2x2V_4.2mm
TI_SN74LVC1G125DCK
TI_SN74AHC1G125DBVR
ADVANTECH
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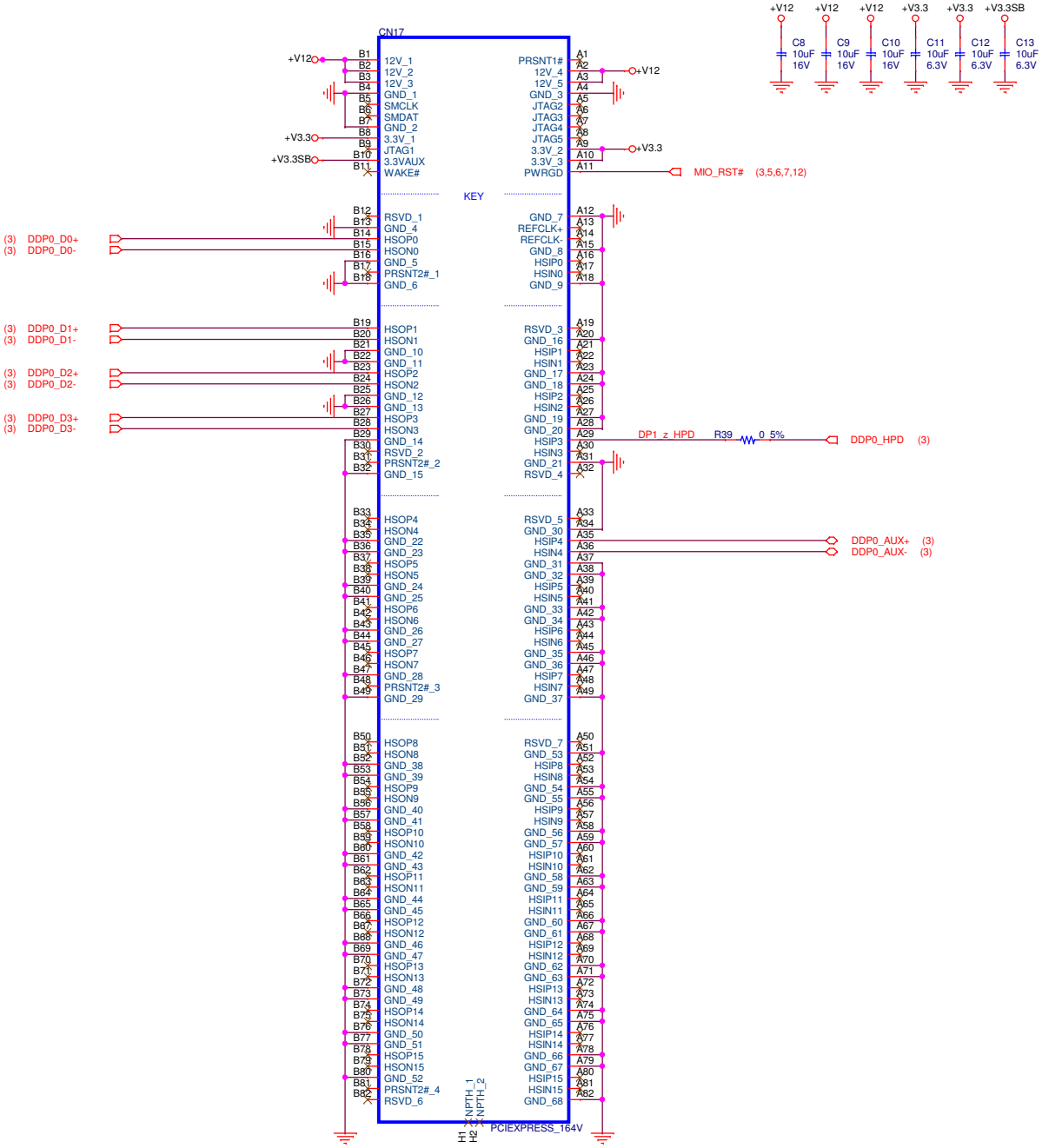

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Title	DisplayPort	
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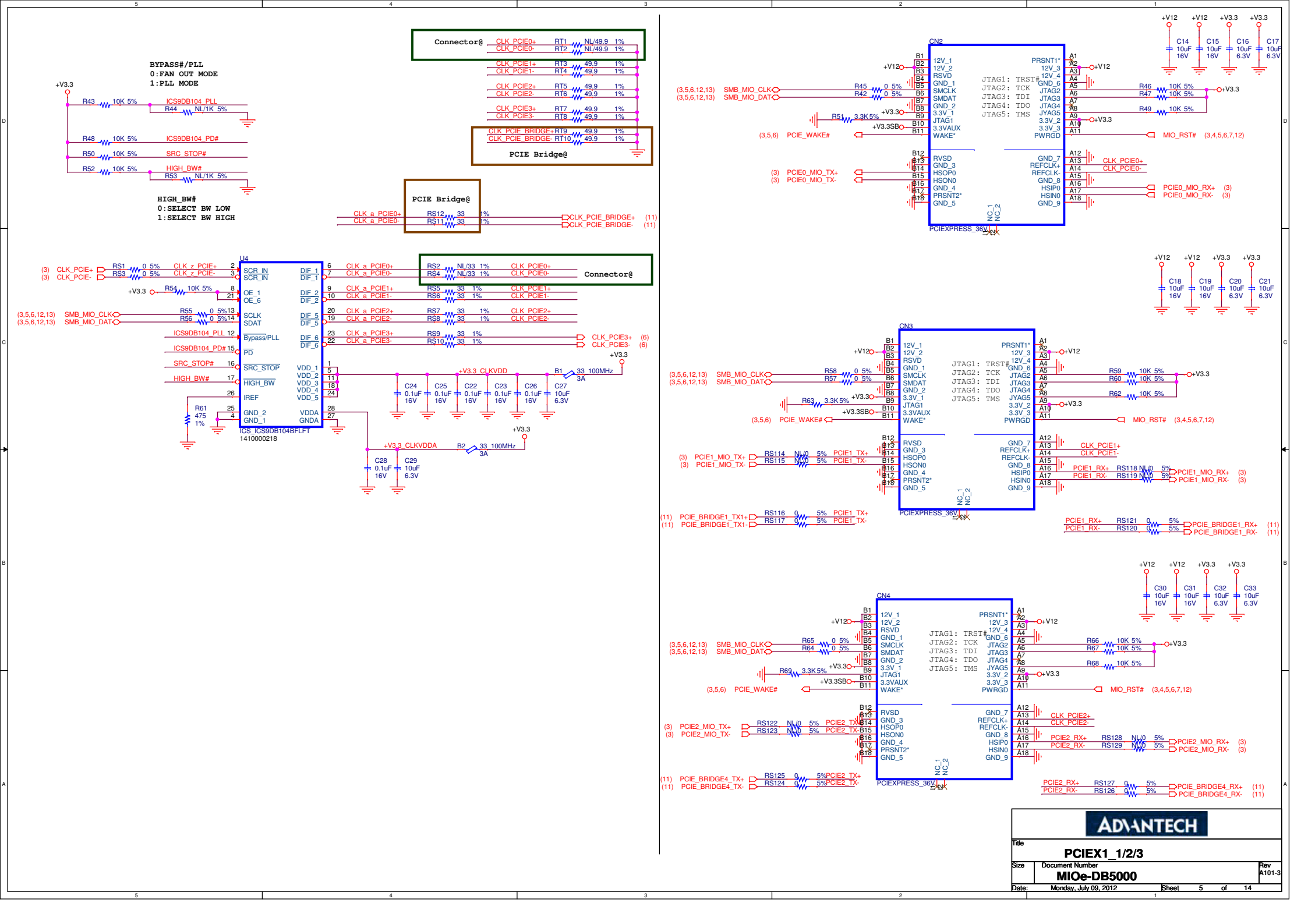
BYPASS#/PLL
0:FAN OUT MODE
1:PLL MODE
HIGH_BW#
0:SELECT BW LOW
1:SELECT BW HIGH
Connector@
PCIE Bridge@
U4
ICS_ICS9DB104BFLFT
1410000218
CN2
CN3
CN4
PCIEXPRESS_36V
Title
PCIEX1_1/2/3
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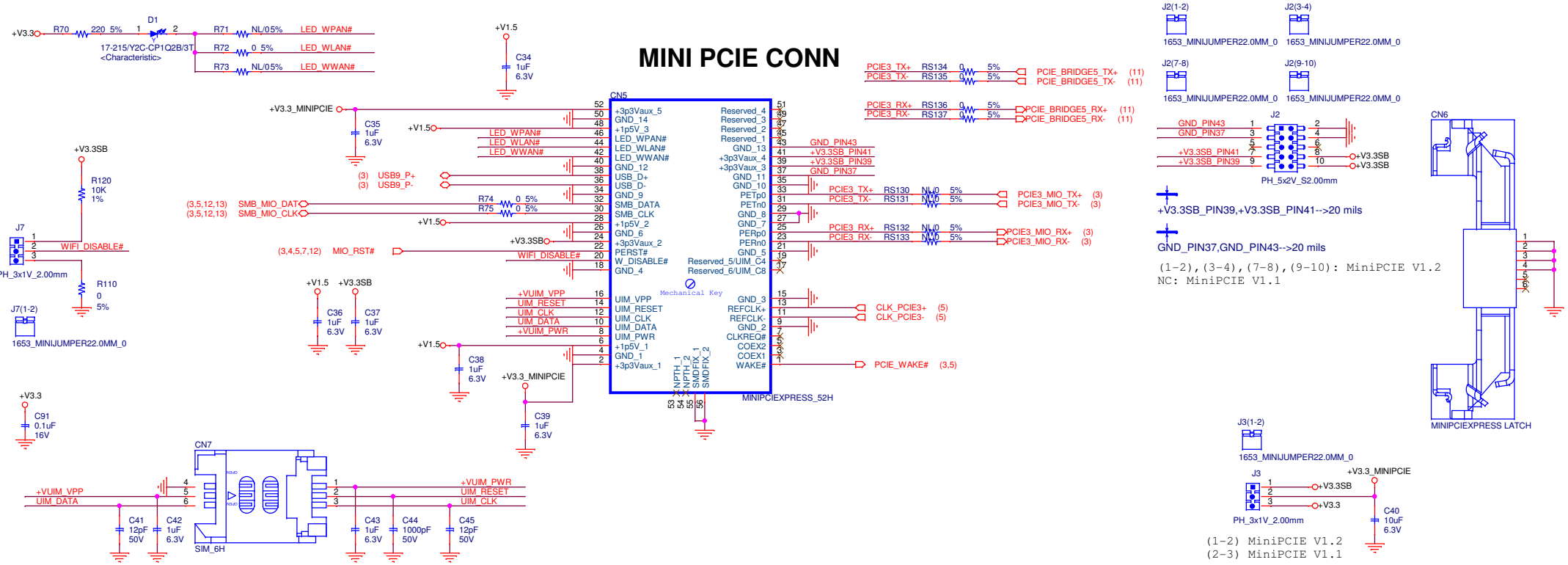

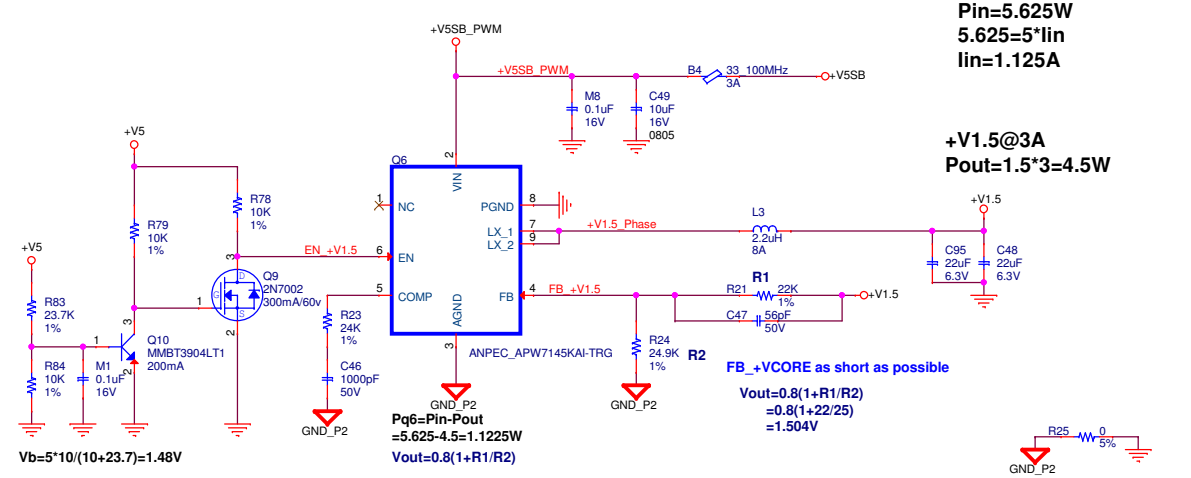

Design note
User Identity Module (UIM) Interface
The UIM signals are defined on the system connector to provide the interface between the removable User Identity Module (UIM), an extension of a Subscriber Identity Module (SIM), and a wireless wide area network (WWAN) radio device residing on the PCI Express Mini Card add-in card. The UIM contains parameters necessary for the WWAN device's operation in a wireless wide area network radio environment.

UIM_PWR (Power source for the UIM): Output
UIM_RESET (UIM reset signal): Output
UIM_CLK (UIM clock signal): Output
UIM_VPP (Variable supply voltage (e.g.,programming voltage) for class A devices): Output
UIM_DATA (UIM data signal): Input/Output

Design note
W_DISABLE# (This signal is used by the system to disable radio operation on add-in cards that implement radio frequency applications): Input
CLKREQ# (is driven low by the PCI Express Mini Card function to request that the PCI Express reference clock be available (active clock state) in order to allow the PCI Express interface to send/receive data)

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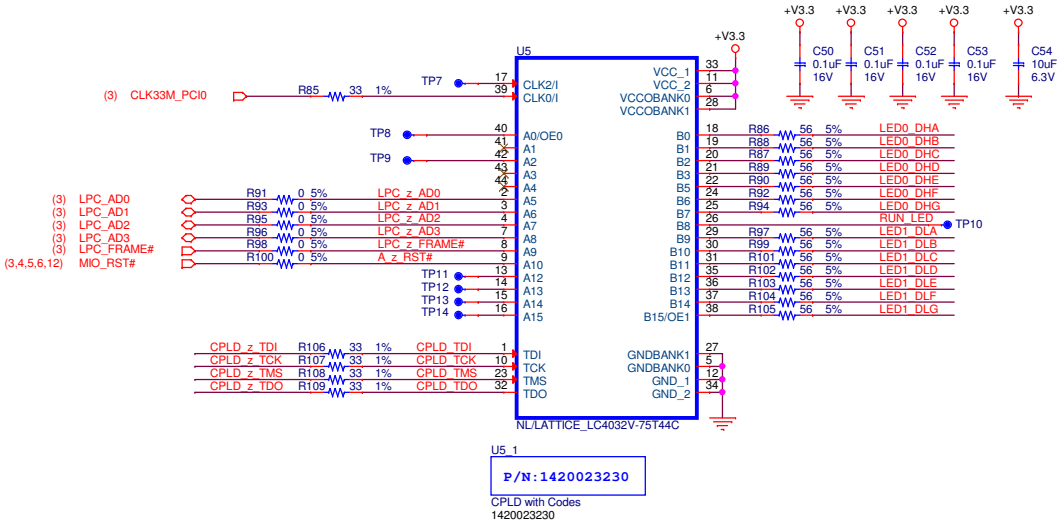
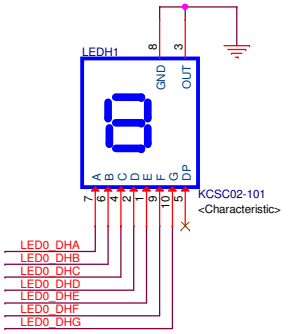
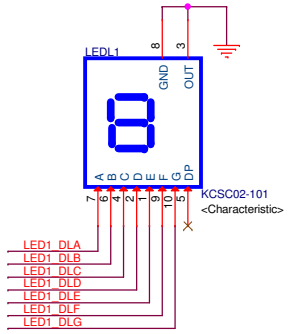
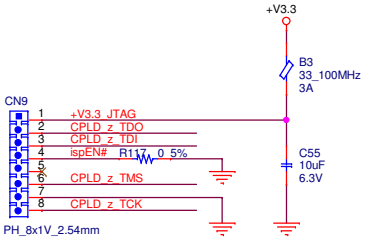
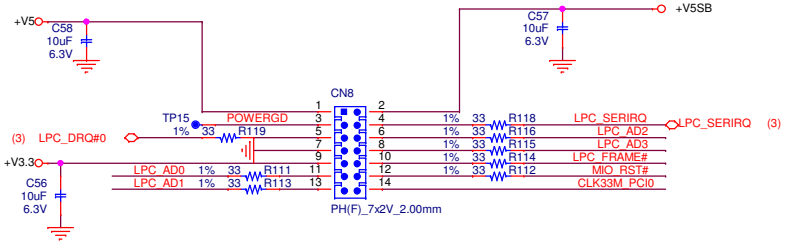








FOR LPC MODULE



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Title	80 PORT/LPC1	
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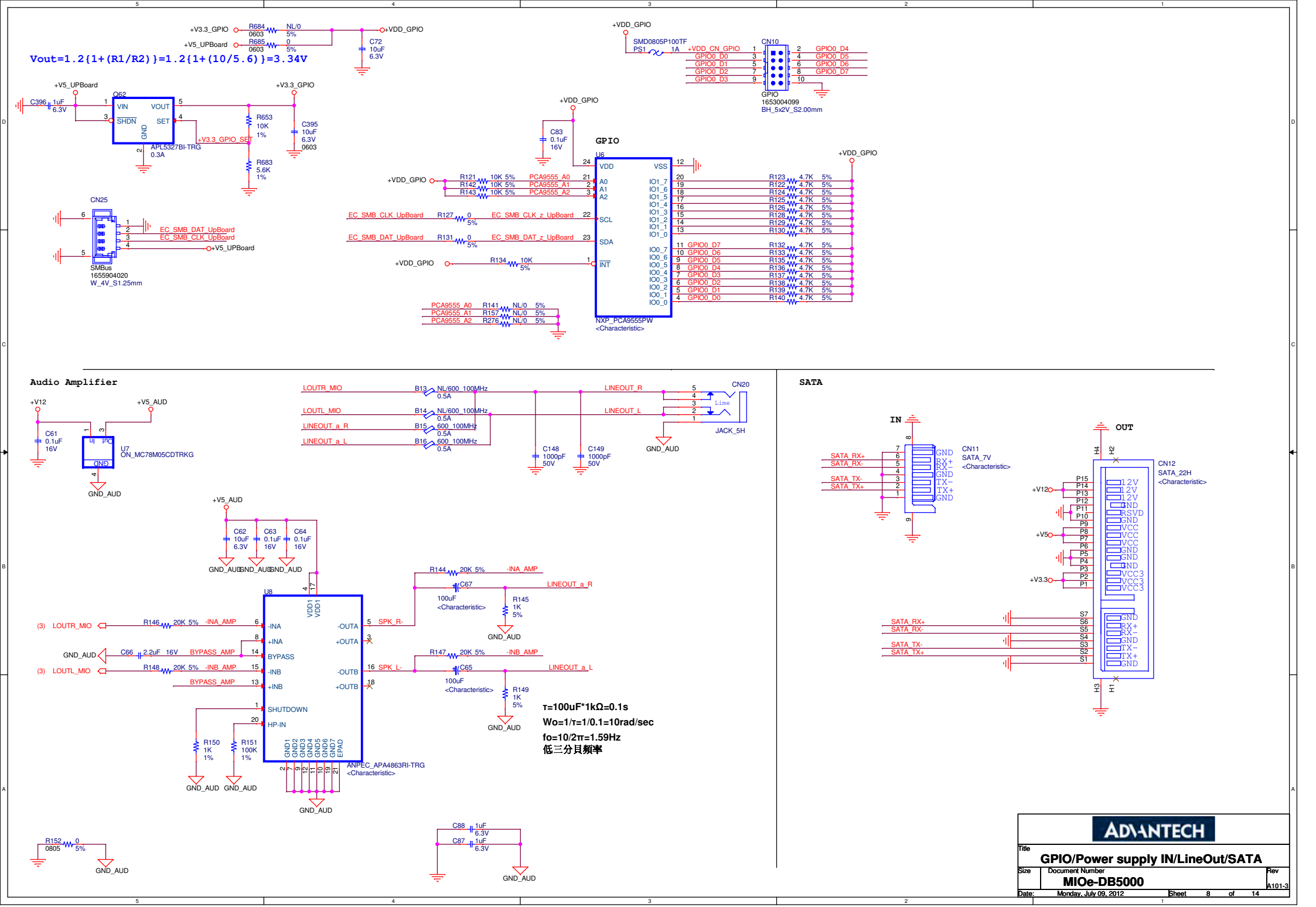

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Title	GPIO/Power supply IN/LineOut/SATA		
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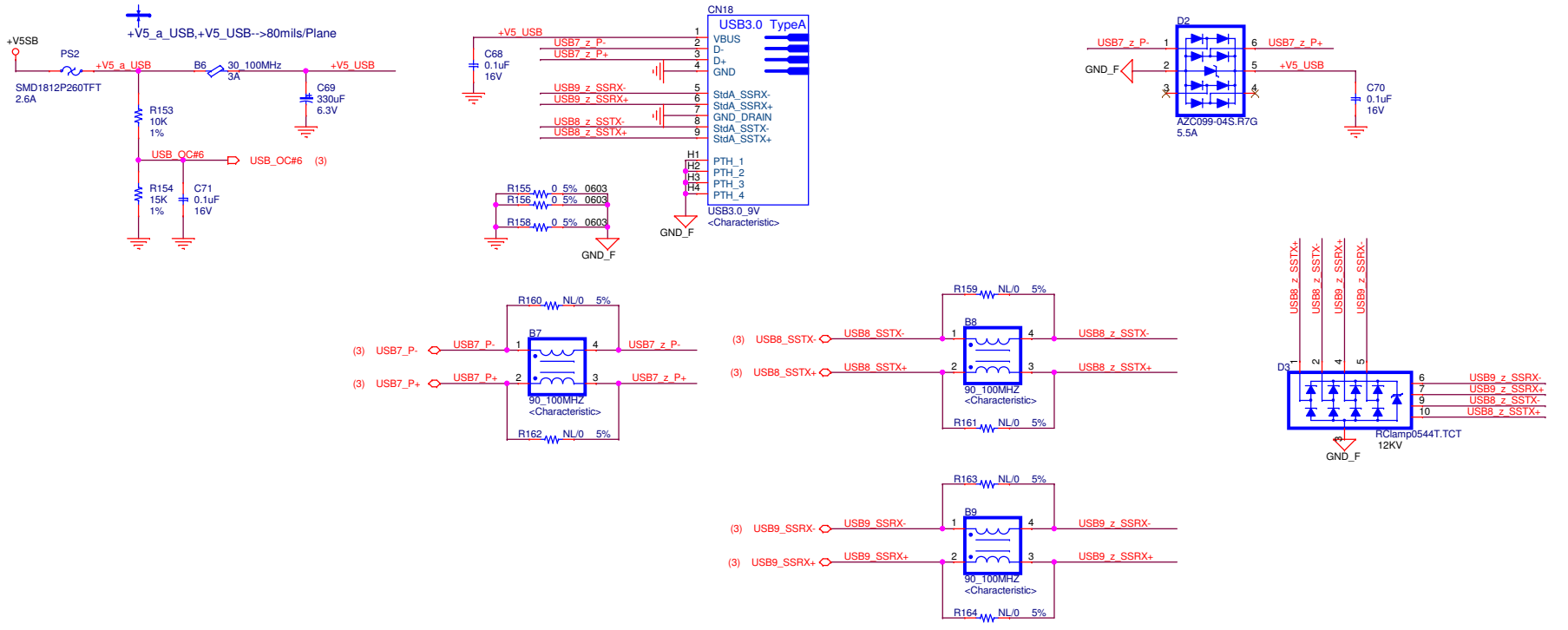

Title	USB 3.0 / 2.0	
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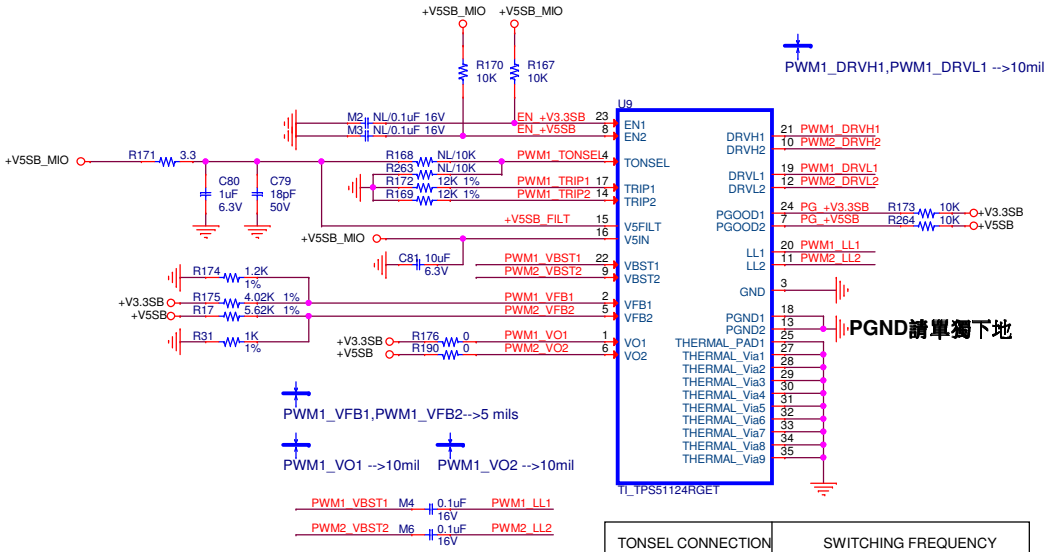


TONSEL CONNECTION	SWITCHING FREQUENCY	
	CH1	CH2
GND	240kHz	300kHz
FLOAT(Open)	*300kHz	360kHz
V5FILT	360kHz	420kHz

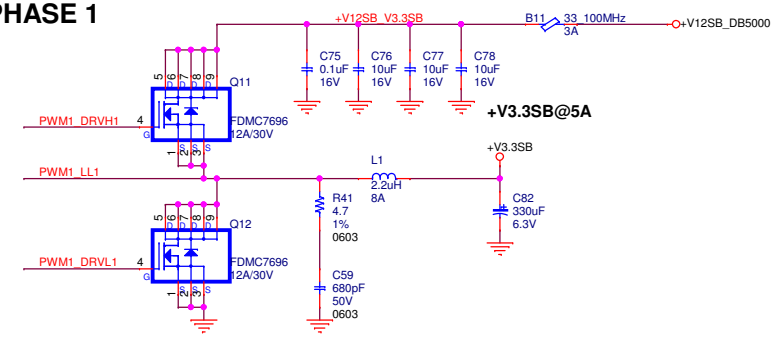
$$V_{trip}(mV) = R_{trip}(k\Omega) \times 10\ (\mu A)$$

$$I_{ocl} = {}^{V_{trip}}/_{R_{DS(on)}} + I_{ripple}/2 = \frac{V_{trip}}{R_{DS(on)}} + \frac{1}{2 \times L \times f} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}}$$

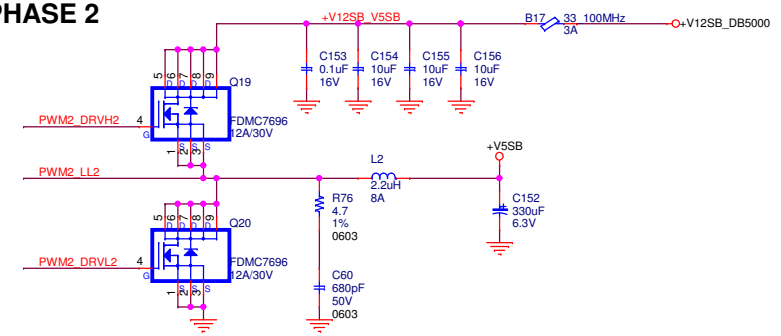
Vout =0.758* (1+R1/R2)
Vout =0.758* (1+4.02/1.2)=3.297
Vout=0.758*(1+5.62/1)=5.01

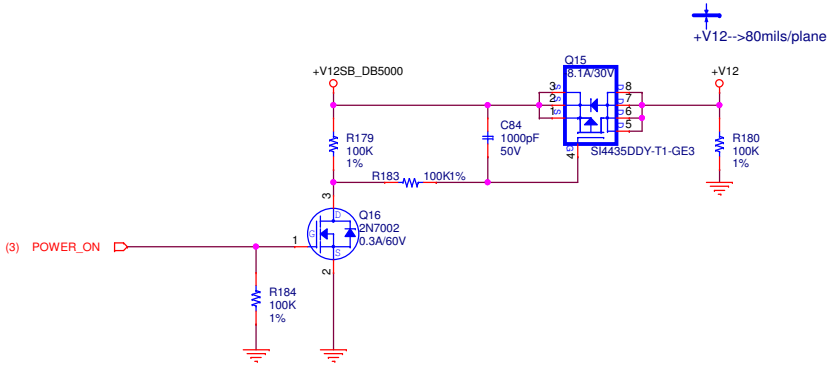
Rdson=14.5mohm,Rtrip=12K,f=300KHz,L=2.2uH
CH1 OCP = 9.1A
Rdson=14.5mohm,Rtrip=12K,f=360KHz,L=2.2uH
CH1 OCP = 8.98A

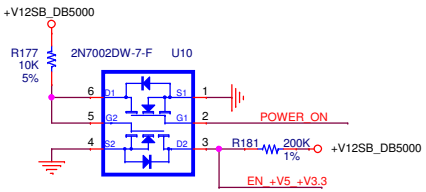
PHASE 1

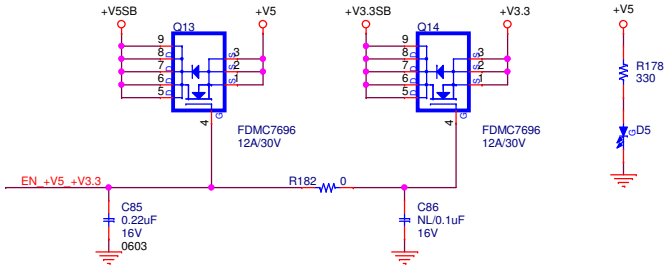


PHASE 2









Title	Power		
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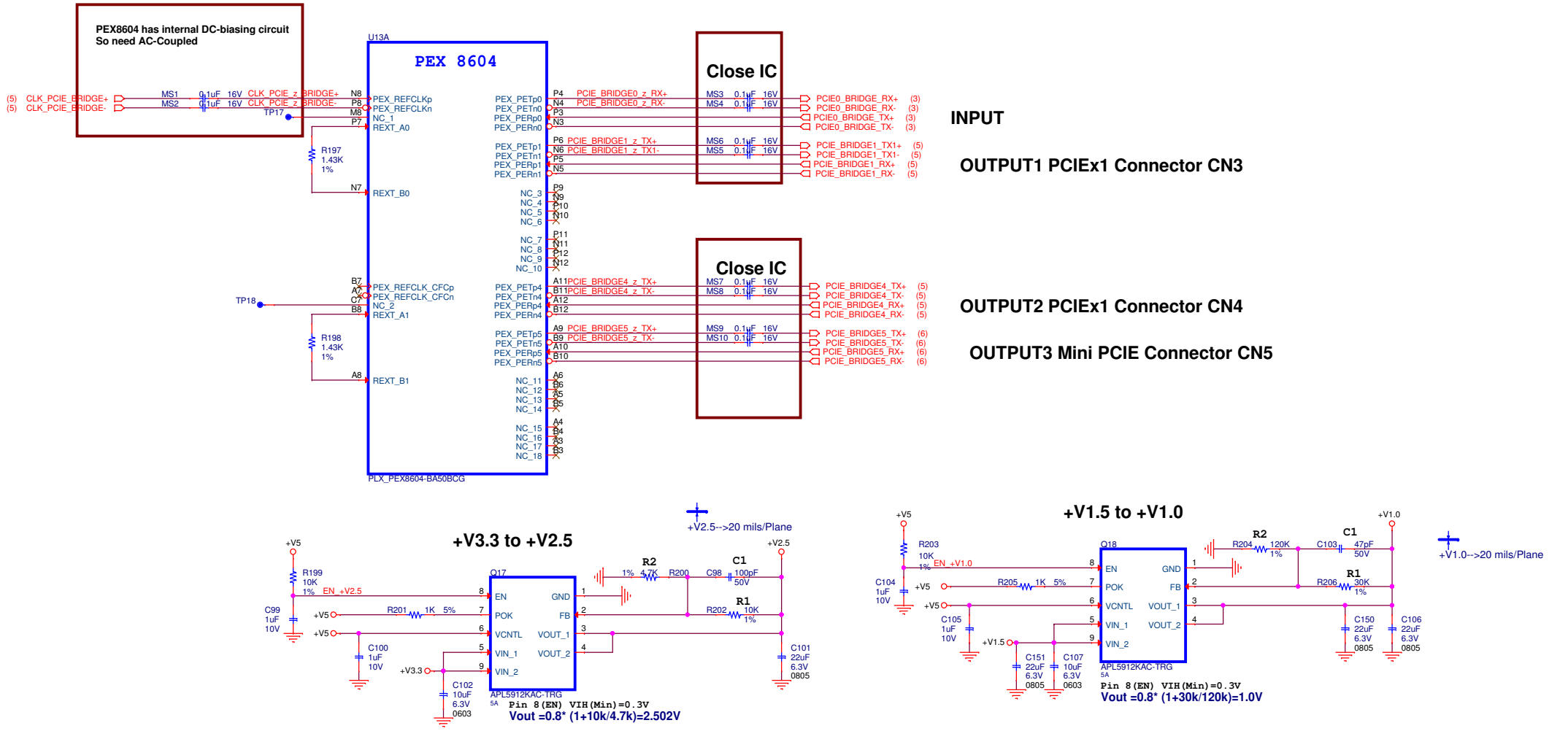

Table 19-4. PEX 8604 Gen 2 (5.0 GT/s) Power Consumption Estimates (Watts)

Lanes	Ports	Core Digital (VDD10) (Amps)		SerDes Analog (VDD10A) (Amps)		SerDes Digital (VDD10) (Amps)		PLL and I/O (VDD25A/VDD25) (Amps)		Total (Watts)	
		Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ[a]	Max[b, c]
4	4	1.00	2.03	0.19	0.31	0.04	0.07	0.02	0.03	1.29	2.61

PCIE BRIDGE TX=>Connector TX B side
PCIE BRIDGE RX=>Connector RX A side

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Title	PCIE BRIDGE	
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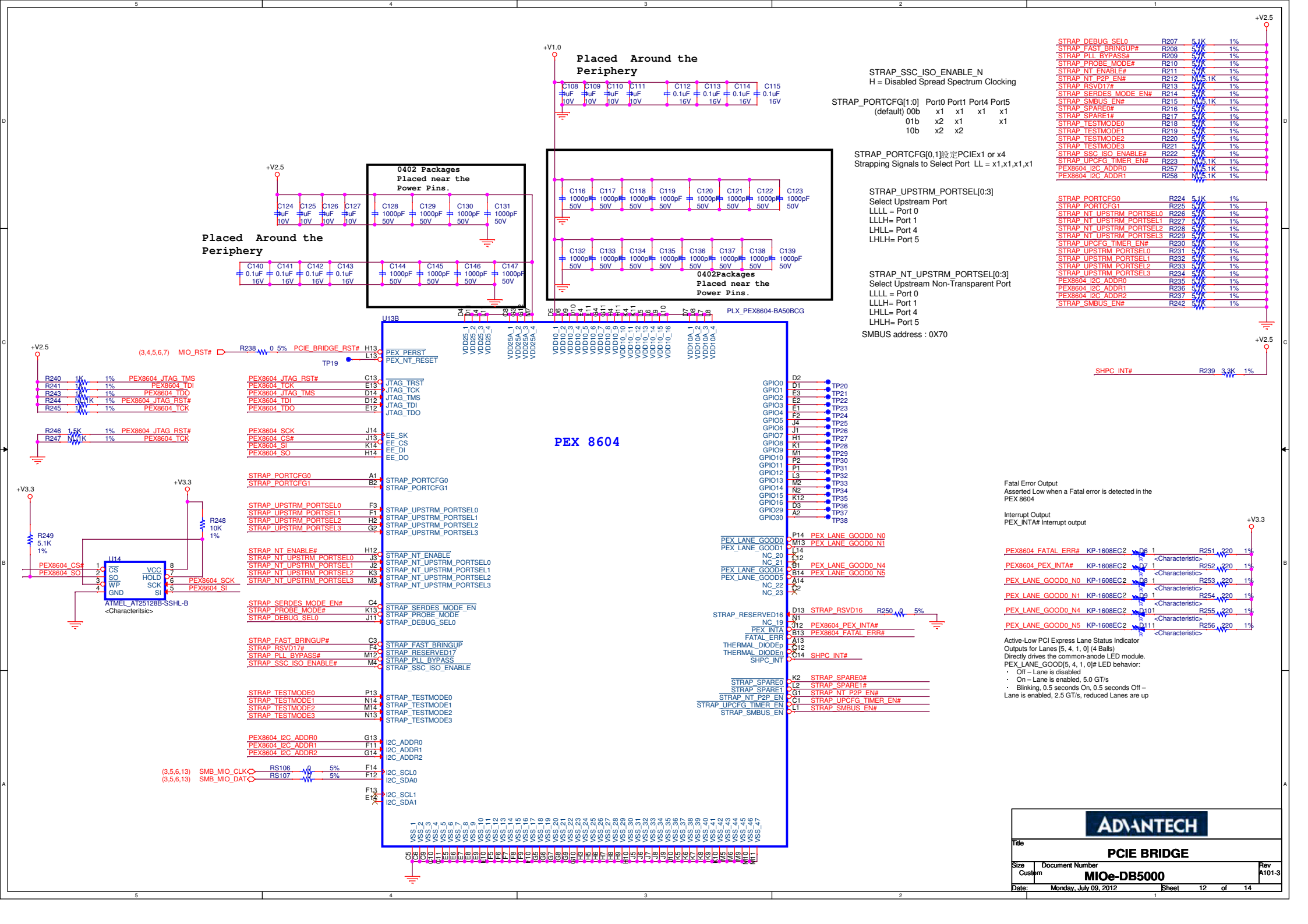
PEX 8604
PLX_PEX8604-BA50BCG
U13B
Placed Around the Periphery
0402 Packages Placed near the Power Pins.
0402Packages Placed near the Power Pins.
STRAP_SSC_ISO_ENABLE_N
H = Disabled Spread Spectrum Clocking
STRAP_PORTCFG[1:0] Port0 Port1 Port4 Port5
(default) 00b x1 x1 x1 x1
01b x2 x1 x1
10b x2 x2
STRAP_PORTCFG[0,1]設定PCIEx1 or x4
Strapping Signals to Select Port LL = x1,x1,x1,x1
STRAP_UPSTRM_PORTSEL[0:3]
Select Upstream Port
LLLL = Port 0
LLLH= Port 1
LHLL= Port 4
LHLH= Port 5
STRAP_NT_UPSTRM_PORTSEL[0:3]
Select Upstream Non-Transparent Port
LLLL = Port 0
LLLH= Port 1
LHLL= Port 4
LHLH= Port 5
SMBUS address : 0X70
Fatal Error Output
Asserted Low when a Fatal error is detected in the PEX 8604
Interrupt Output
PEX_INTA# Interrupt output
Active-Low PCI Express Lane Status Indicator Outputs for Lanes [5, 4, 1, 0] (4 Balls)
Directly drives the common-anode LED module.
PEX_LANE_GOOD[5, 4, 1, 0]# LED behavior:
· Off – Lane is disabled
· On – Lane is enabled, 5.0 GT/s
· Blinking, 0.5 seconds On, 0.5 seconds Off – Lane is enabled, 2.5 GT/s, reduced Lanes are up
A1MEL_AT25128B-SSHL-B
<Characteritsic>
ADVANTECH
Title
PCIE BRIDGE
Size Custom
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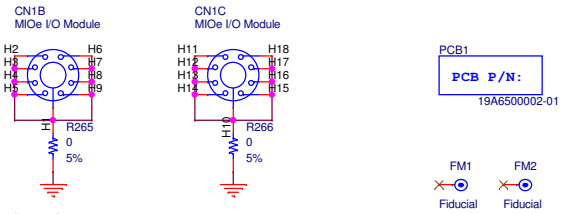
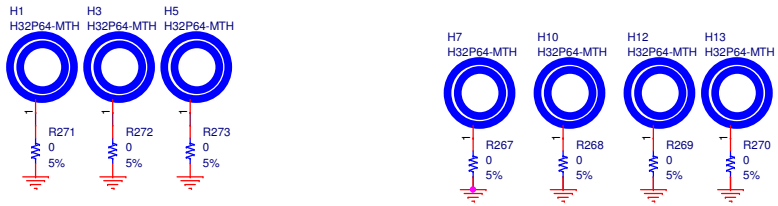
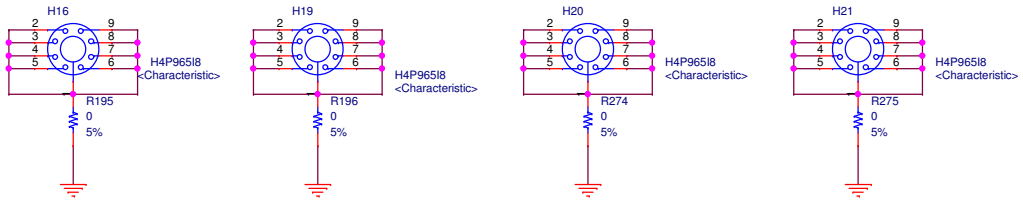
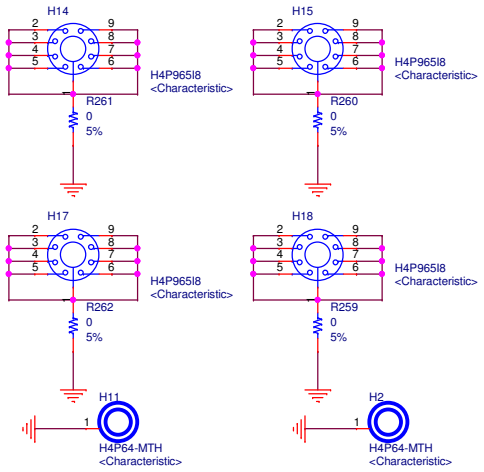


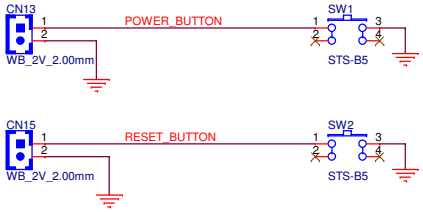
9696D50000E=ASS'Y MIOe-DB5000 A101-1 Carrier board
9696D50001E=ASS'Y MIOe-DB5000 A101-1 with PCIe Bridge







Power & Reset Button



SMBus Connector

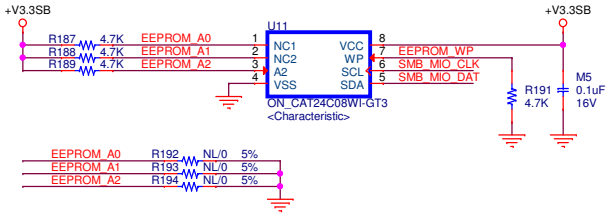


Table 5-1: PCI Express Connectors Pinout

Pin #	Side B		Side A	
	Name	Description	Name	Description
1	+12V	12 V power	PRSNT1#	Hot-Plug presence detect
2	+12V	12 V power	+12V	12 V power
3	+12V	12 V power	+12V	12 V power
4	GND	Ground	GND	Ground
5	SMCLK	SMBus (System Management Bus) clock	JTAG2	TCK (Test Clock), clock input for JTAG interface
6	SMDAT	SMBus (System Management Bus) data	JTAG3	TDI (Test Data Input)
7	GND	Ground	JTAG4	TDO (Test Data Output)
8	+3.3V	3.3 V power	JTAG5	TMS (Test Mode Select)
9	JTAG1	TRST# (Test Reset) resets the JTAG interface	+3.3V	3.3 V power
10	3.3Vaux	3.3 V auxiliary power	+3.3V	3.3 V power
11	WAKE#	Signal for Link reactivation	PERST#	Fundamental reset

Pin #	Side B		Side A	
	Name	Description	Name	Description
Mechanical key				
12	RSVD	Reserved	GND	Ground
13	GND	Ground	REFCLK+	Reference clock (differential pair)
14	PETp0	Transmitter differential pair, Lane 0	REFCLK-	
15	PETn0		GND	Ground
16	GND	Ground	PERp0	Receiver differential pair, Lane 0
17	PRSNT2#	Hot-Plug presence detect	PERn0	
18	GND	Ground	GND	Ground
End of the x1 connector				

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MIOe-DB5000 Revision History

MIOe-DB5000 REV.A101-1 PCB:19A6500000 96 BOM:9696D50000E 9696D50001E

none

MIOe-DB5000 REV.A101-2 PCB:19A6500001 96 BOM:9696D50000E 9696D50001E

1.Follow ME request modify PCB size.

MIOe-DB5000 REV.A101-3 PCB:19A6500002-01 96 BOM:9696D50000E 9696D50001E

1.Change C85 to 0.22uf
2.Change R181 from 20k to 200k
3.Change R223 to NL
4.Pop R230
5.change U11 to 1410022246 ,because old part EOL
6.For LDO thermal issue , change +V3.3 to +V1.5 solution to ANPEC_APW7145KAI-TRG

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