ADVANTECH

Enabling an Intelligent Planet

MI/O-128™ Single Board Computer
Design Guide

V1.0
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Chap. 1 I/O 128 Pin

MIO series feature two 64-pin connectors, which one is DIP type and another is SMD type, for I/O extension, refer to Figure 1-1. This interface, including power input, inverter output, VGA, USB 2.0, GPIO and RS-232, can implement low speed functions directly. This chapter will show all the pin description.

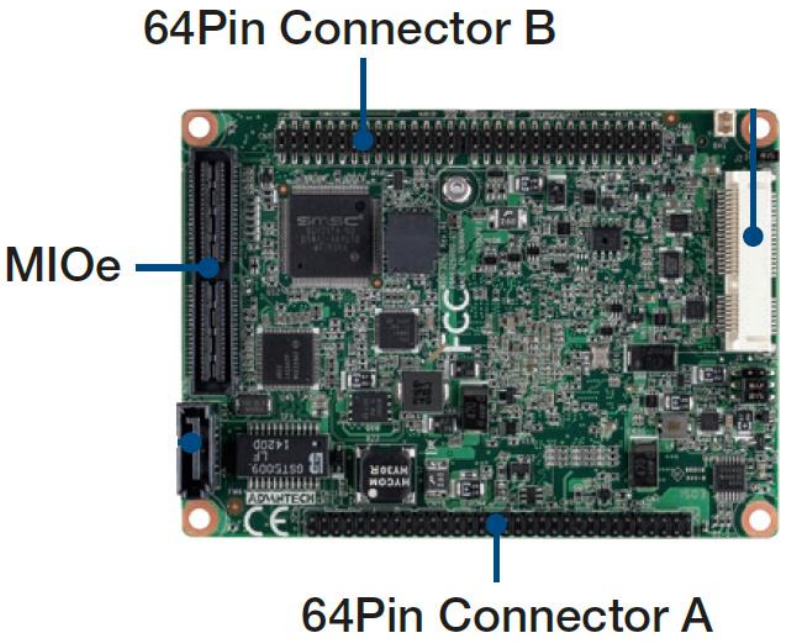


Figure 1-1 DIP 64-Pin Connector A & SMD 64-Pin Connector B

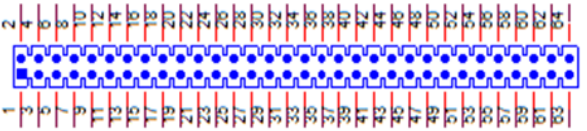


Figure 1-2 DIP 64-Pin Connector Symbol

Pin	Name	Pin	Name
1	12V Input	2	GND
3	12V Input	4	GND
5	12V Input	6	GND
7	12V Input	8	GND
9	GND	10	GND
11	GND	12	GND
13	Inverter 5V Output	14	GND
15	Inverter ENBKL	16	Inverter VBR
17	Inverter 12V Output	18	GND
19	GND	20	GND
21	GND	22	GND
23	VGA DDC DAT	24	VGA DDC CLK
25	VGA RGB GND	26	VGA RGB GND
27	VGA Red	28	VGA Green
29	VGA Blue	30	VGA RGB GND
31	VGA GND	32	VGA 5V Output
33	VGA HSYNC	34	VGA VSYNC
35	GND	36	GND
37	GND	38	GND
39	USB 5V Output	40	USB 5V Output
41	USB0 D-	42	USB1 D-

43	USB0 D+	44	USB1 D+
45	GND	46	GND
47	USB Chassis GND	48	NC
49	GND	50	GND
51	LAN LINK100 LED-	52	LAN LINK1000 LED-
53	LAN ACT LED+	54	LAN ACT LED-
55	LAN BI_DA+	56	LAN BI_DA-
57	LAN BI_DB+	58	LAN BI_DB-
59	LAN BI_DC+	60	LAN BI_DC-
61	LAN BI_DD+	62	LAN BI_DD-
63	LAN Chassis GND	64	LAN Chassis GND

Table 1-1 Pin Description of DIP 64-Pin Connector

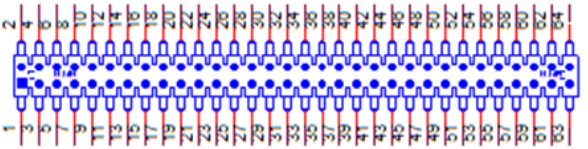


Figure 1-3 SMD 64-Pin Connector Symbol

Pin	Name	Pin	Name
1	Power Button Pin1	2	Power LED+
3	Power Button Pin2	4	Power LED-
5	Reset Button Pin1	6	HDD LED+
7	Reset Button Pin2	8	HDD LED-
9	GND	10	SMB 5V Output
11	SMB DAT	12	SMB CLK
13	I2C DAT	14	I2C CLK
15	GPIO 5VSB Output	16	GPIO4
17	GPIO0	18	GPIO5
19	GPIO1	20	GPIO6
21	GPIO2	22	GPIO7
23	GPIO3	24	GND
25	USB 5V Output	26	USB 5V Output
27	USB0 D-	28	USB1 D-
29	USB0 D+	30	USB1 D+
31	GND	32	GND
33	USB Chassis GND	34	NC
35	AUDIO LOUTR	36	AUDIO LINR
37	AUDIO GND	38	AUDIO GND
39	AUDIO LOUTL	40	AUDIO LINL
41	AUDIO GND	42	AUDIO GND
43	AUDIO MICR	44	AUDIO MICL

45	COM1 422TX-/485D-/DCD#	46	COM1 DSR#
47	COM1 422TX+/485D+/RXD	48	COM1 RTS#
49	COM1 422RX+/TXD	50	COM1 CTS#
51	COM1 422RX-/DTR#	52	COM1 RI#
53	GND	54	GND
55	COM2 422TX-/485D-/DCD#	56	COM2 DSR#
57	COM2 422TX+/485D+/RXD	58	COM2 RTS#
59	COM2 422RX+/TXD	60	COM2 CTS#
61	COM2 422RX-/DTR#	62	COM2 RI#
63	GND	64	GND

Table 1-2 Pin Description of SMD 64-Pin Connector

1.1 Audio

The HD Audio, which can provide DAC channels to support LOUT and stereo ADCs to support stereo MIC and LIN, is established on the CPU board. The audio signal MICL, MICR, LINL, LINR, LOUTL, LOUTR and AGND are the interface for audio application.

1.1.1 Signal Description

SMD Pin	Name	Pin Type	Power Rail	Description
35	AUDIO LOUTR	Output	1.2Vrms	LINE-R Output
37	AUDIO GND	Audio GND	Audio GND	Audio GND
39	AUDIO LOUTL	Output	1.2Vrms	LINE-L Output
41	AUDIO GND	Audio GND	Audio GND	Audio GND
43	AUDIO MICR	Input	1.5Vrms	MIC-R Input
36	AUDIO LINR	Input	1.5Vrms	LINE-R Input
38	AUDIO GND	Audio GND	Audio GND	Audio GND
40	AUDIO LINL	Input	1.5Vrms	LINE-L Input
42	AUDIO GND	Audio GND	Audio GND	Audio GND

Table 1.1.1-1 Signal Description for Audio

1.1.2 Schematic Guidelines

AGND is clear analog ground for audio, and all the audio signals should refer to it in CPU board. What's more, one 0 ohm resistor for the return path connects the signal GDN with the audio AGND in CPU board. Considering EMI, the bead and capacitors are the recommendatory solution. For placement concern, EMI solution should be close to connector.

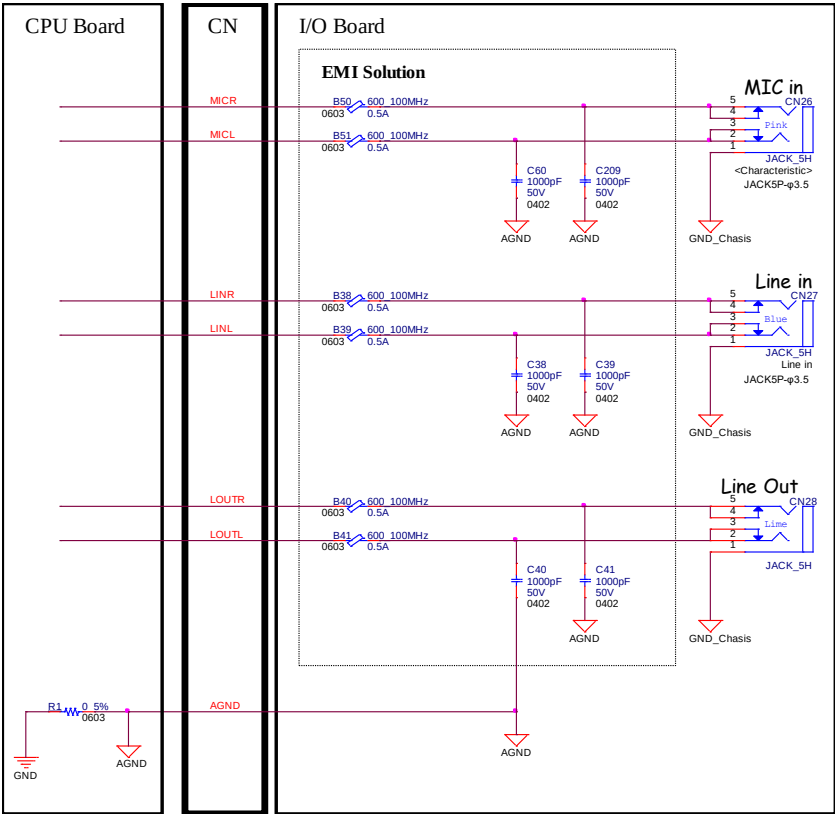


Figure 1.1.1-1 Audio Application

1.2 VGA

This interface can support one VGA port for display, and is compatible with WESA. As for the detail, users need to confirm CPU board manual first because the real specifications are based on chipsets.

1.2.1 Signal Descriptions

DIP Pin	Name	Pin Type	Power Rail	Description
23	VGA DDC DAT	I/O	5V	VGA DDC Data
25	VGA RGB GND	Analog GND	Analog GND	VGA RGB Ground
27	VGA Red	Output	0.7Vp-p	Red Analog Video Output
29	VGA Blue	Output	0.7Vp-p	Blue Analog Video Output
31	VGA GND	GND	GND	GND
33	VGA HSYNC	Output	3.3V	VGA Hsync Output
24	VGA DDC CLK	I/O	5V	VGA DDC Clock
26	VGA RGB GND	GND	Analog GND	VGA RGB Ground
28	VGA Green	Output	0.7Vp-p	Green Analog Video Output
30	VGA RGB GND	GND	Analog GND	VGA RGB Ground
32	VGA 5V Output	Power Output	5V	Power output for VGA (500mA)
34	VGA VSYNC	Output	3.3V	VGA Vsync Output

Table 1.2.1-1 Signal Description for VGA

1.2.2 Schematic Guidelines

Each RGB output (RED, GREEN, and BLUE) is terminated with one 150-Ω resistor near the chipset from the DAC output to the board ground. A second 150Ω resistor should be placed close to the CRT connector. Additionally, one 75-Ω termination resistor exists within the display. The equivalent DC resistance at the output of each DAC is 37.5 Ω. The current output from each DAC flows into this equivalent resistive load to produce a video voltage without the need for external buffering. There is also a pi-filter on each channel that is used to reduce high-frequency noise and to reduce EMI. In order to maximize the performance, the filter impedance, cable impedance, and load impedance should be matched.

The host VGA controller in CPU board is weak device without strong ESD protection, and therefore ESD and EMI solutions close to connector are must for VGA port.

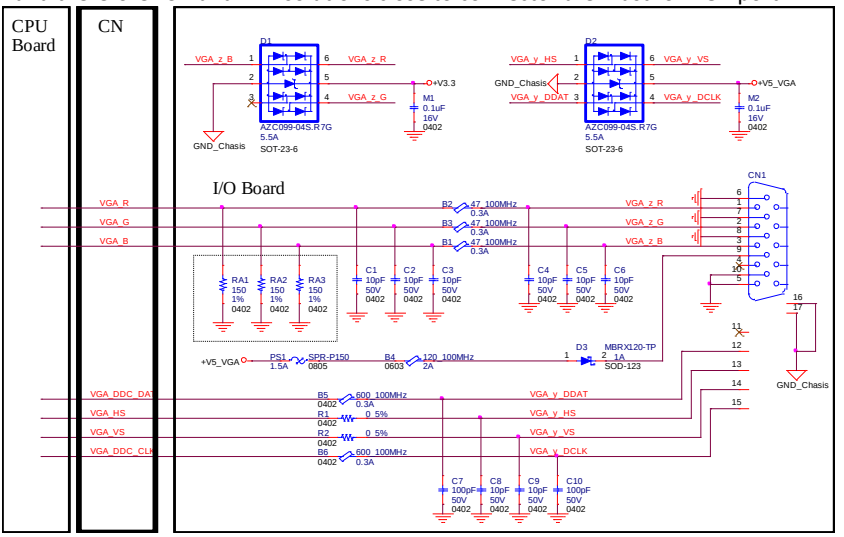


Figure 1.2.1-1 Demonstration for VGA Application

1.3 USB

This interface can support USB 2.0 up to 4 ports, and four power pins which are with current rating up to 500mA per pin. USB ports can support high-speed (HS), full-speed (FS), and low-speed (LS) traffic. In addition, it features backward compatible to USB specification Revision 1.1, and support low speed I/O USB devices, such as keyboard and mouse.

1.3.1 Signal Descriptions

DIP Pin	Name	Pin Type	Power Rail	Description
39	USB 5V Output	Power Output	5VSB	USB Power(500mA)
41	USB0 D-	I/O USB2		USB2 Data-
43	USB0 D+	I/O USB2		USB2 Data+
45	GND	GND	GND	GND
47	USB Chassis GND	GND	GND	GND
40	USB 5V Output	Power Output	5V	USB Power(500mA)
42	USB1 D-	I/O USB2		USB2 Data-
44	USB1 D+	I/O USB2		USB2 Data+
46	GND	GND	GND	GND
48	NC			

Table 1.3.1-1 Signal Description for USB in DIP 64-Pin

SMD Pin	Name	Pin Type	Power Rail	Description
25	USB 5V Output	Power Output	5VSB	USB Power(500mA)
27	USB0 D-	I/O USB2		USB2 Data-
29	USB0 D+	I/O USB2		USB2 Data+
31	GND	GND	GND	GND
33	USB Chassis GND	GND	GND	GND
26	USB 5V Output	Power Output	5VSB	USB Power(500mA)

28	USB1 D-	I/O USB2		USB2 Data-
30	USB1 D+	I/O USB2		USB2 Data+
32	GND	GND	GND	GND
34	NC			

Table 1.3.1-2 Signal Description for USB in SMD 64-Pin

1.3.2 Schematic Guidelines

Considering EMI and ESD issue, the common mode choke and TVS (Transient Voltage Suppression) diode with low capacitance, which should be less than 1.0pF, are the recommendatory solution. For placement concern, EMI and ESD solution should be close to connector.

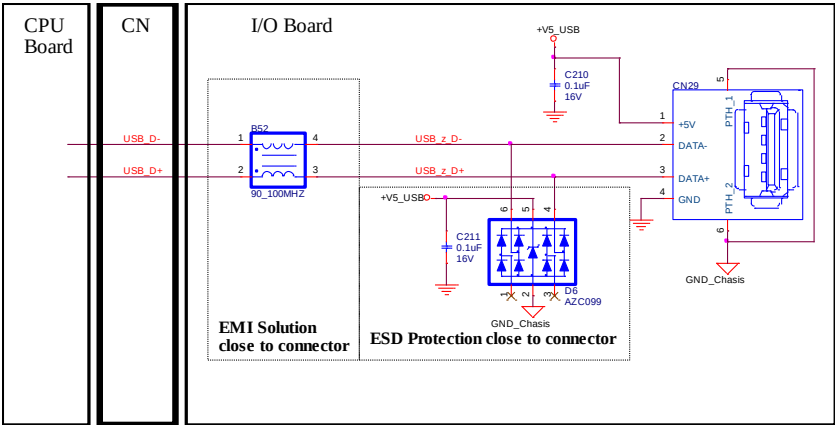


Figure 1.3.2-1 EMI and ESD demonstration for USB Application

1.4 COM

This interface can support RS-232 up to 4 ports and RS-422/485 up to 2 ports share with RS-232. The transmitters/receivers of RS-232/422/485, which integrate ESD protection, can reduce external ESD components. All the port functions can be configured by BIOS setting before users make use of this interface.

1.4.1 Signal Descriptions

SMD Pin	Name	Pin Type	Power Rail	Description
45	COM1 422TX-/485D-/DCD#	Refer to RS232/RS422/RS485 Standard	Refer to RS232/RS422/RS485 Standard	422TX-/485D-/DCD#
47	COM1 422TX+/485D+/RXD			422TX+/485D+/RXD
49	COM1 422RX+/TXD			422RX+/TXD
51	COM1 422RX-/DTR#			422RX-/DTR#
53	GND	GND	GND	GND
55	COM2 422TX-/485D-/DCD#	Refer to RS232/RS422/RS485 Standard	Refer to RS232/RS422/RS485 Standard	422TX-/485D-/DCD#
57	COM2 422TX+/485D+/RXD			422TX+/485D+/RXD
59	COM2 422RX+/TXD			422RX+/TXD
61	COM2 422RX-/DTR#			422RX-/DTR#
63	GND	GND	GND	GND
46	COM1 DSR#	Refer to RS232/RS422/RS485 Standard	Refer to RS232/RS422/RS485 Standard	DSR#
48	COM1 RTS#			RTS#
50	COM1 CTS#			CTS#
52	COM1 RI#			RI#
54	GND	GND	GND	GND
56	COM2 DSR#	Refer to RS232/RS422/RS485 Standard	Refer to RS232/RS422/RS485 Standard	DSR#
58	COM2 RTS#			RTS#
60	COM2 CTS#			CTS#

62	COM2 RI#			RI#
64	GND	GND	GND	GND

Table 1.4.1-1 Signal Description for COM

1.4.2 Schematic Guidelines

As for general ESD protection, the transmitters/receivers of RS-232/422/485 in CPU board can meet the requirement, and users don't implement extra ESD components. Considering EMI, the bead and capacitors are the recommendatory solution. For placement concern, EMI solution should be close to connector.

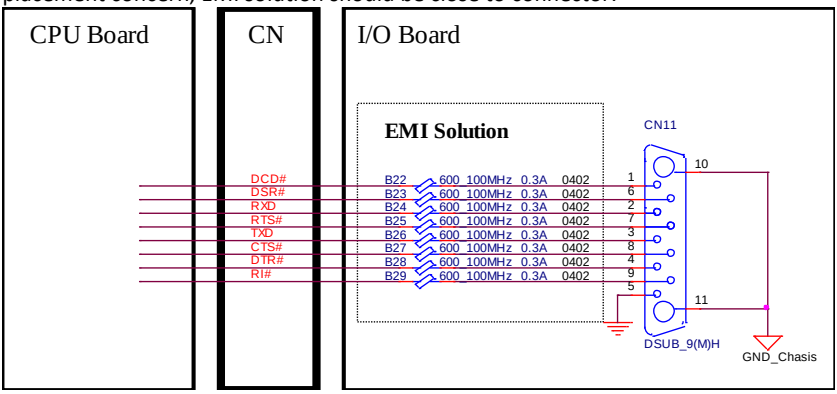


Figure 1.4.2-1 EMI demonstration for RS-232 Application

1.5 LAN

One LAN port in this interface enables 1000BASE-T implementations using an integrated PHY and transformer in CPU board, and therefore one RJ45 connector without transformer can complete the Ethernet application. In addition, linking and active LED functions can indicate LAN port status for front panel in system.

1.5.1 Signal Descriptions

DIP Pin	Name	Pin Type	Pwr Rail	Description
51	LAN LINK100 LED-	Define by LAN Chip	3.3V	100Mb/s LED
53	LAN ACT LED+	Define by LAN Chip	3.3V	LAN Active LED
55	LAN BI_DA+	I/O		DATA A+
57	LAN BI_DB+	I/O		DATA B+
59	LAN BI_DC+	I/O		DATA C+
61	LAN BI_DD+	I/O		DATA D+
63	LAN Chassis GND	GND	GND	GND
52	LAN LINK1000 LED-	Define by LAN Chip	3.3V	1000Mb/s LED
54	LAN ACT LED-	Define by LAN Chip	3.3V	LAN Active LED
56	LAN BI_DA-	I/O		DATA A-
58	LAN BI_DB-	I/O		DATA B-
60	LAN BI_DC-	I/O		DATA C-
62	LAN BI_DD-	I/O		DATA D-
64	LAN Chassis GND	GND	GND	GND

Table 1.5.1-1 Signal Description for COM

1.5.2 Schematic Guidelines

For Ethernet application, RJ45 connector is the only component. Additionally, all differential pairs routing with differential impedance 100 ohm for signals BI_DA+/-, BI_DB+/-, BI_DC+/- and BI_DD+/- in I/O board PCB connect with DIP 64-Pin and RJ45 connectors directly.

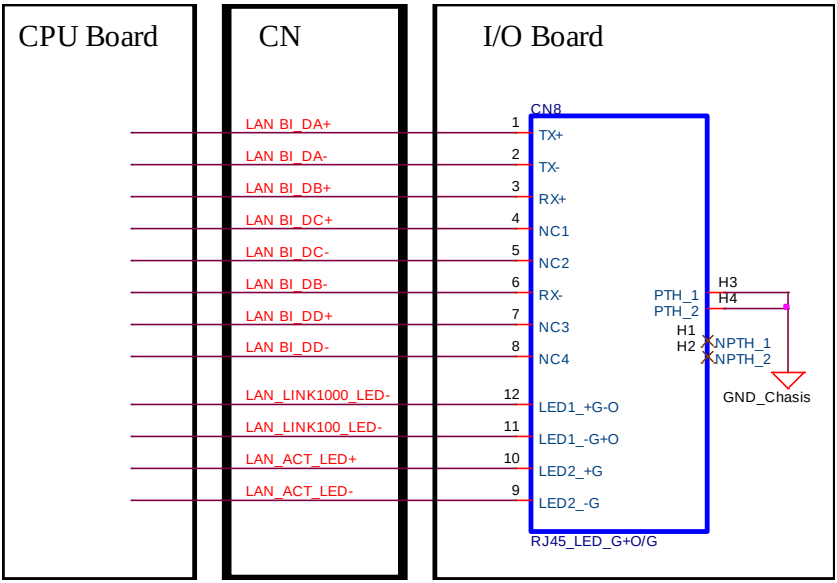


Figure 1.5.2-1 Demonstration for LAN Application

1.6 Others

The other functions in this interface are power input, inverter, front panel, SMBus, I2C, LEDs, and GPIO.

1.6.1 Signal Descriptions

DIP Pin	Name	Pin Type	Power Rail	Description
1	12V Input	Power Input	12V	Power input for MB.
3	12V Input	Power Input	12V	Power input for MB.
5	12V Input	Power Input	12V	Power input for MB.
7	12V Input	Power Input	12V	Power input for MB.
9	GND	GND	GND	GND
11	GND	GND	GND	GND
13	Inverter 5V Output	Power Output	5V	Power output for Inverter Board.(1A)
15	Inverter ENBKL	Output	5V	LCD Panel Backlight Enable
17	Inverter 12V Output	Power Output	12V	Power output for Inverter Board.(500mA)
19	GND	GND	GND	GND
21	GND	GND	GND	GND
2	GND	GND	GND	GND
4	GND	GND	GND	GND
6	GND	GND	GND	GND
8	GND	GND	GND	GND
10	GND	GND	GND	GND
12	GND	GND	GND	GND
14	GND	GND	GND	GND
16	Inverter VBR	Output	5V	PWM Output for Backlight Brightness
18	GND	GND	GND	GND
20	GND	GND	GND	GND

22	GND	GND	GND	GND

Table 1.6.1-1 Signal Description for Others in DIP 64-Pin

SMD Pin	Name	Pin Type	Power Rail	Description
1	Power Button Pin1	Input	3.3VSB	Power Button
3	Power Button Pin2	GND	GND	GND
5	Reset Button Pin1	Input	3.3V	Reset Button
7	Reset Button Pin2	GND	GND	GND
9	GND	GND	GND	GND
11	SMB DAT	I/O	5V	SMBus Data
13	I2C DAT	I/O	5V	I2C Data
15	GPIO 5VSB Output	Power Output	5VSB	Power output for GPIO. (500mA)
17	GPIO0	I/O	5VSB	GPIO (with Internal pull up to 5VSB)
19	GPIO1	I/O	5VSB	GPIO (with Internal pull up to 5VSB)
21	GPIO2	I/O	5VSB	GPIO (with Internal pull up to 5VSB)
23	GPIO3	I/O	5VSB	GPIO (with Internal pull up to 5VSB)
2	Power LED+	LED+	5V	Power LED
4	Power LED-	GND	GND	Power LED
6	HDD LED+	LED+	3.3V	HDD LED
8	HDD LED-	LED-	3.3V	HDD LED
10	SMB 5V Output	Power Output	5V	Power output for SMBus.(500mA)
12	SMB CLK	I/O	5V	SMB Clock
14	I2C CLK	I/O	5V	I2C Clock
16	GPIO4	I/O	5VSB	GPIO (with Internal pull up to 5VSB)

18	GPIO5	I/O	5VSB	GPIO (with Internal pull up to 5VSB)
20	GPIO6	I/O	5VSB	GPIO (with Internal pull up to 5VSB)
22	GPIO7	I/O	5VSB	GPIO (with Internal pull up to 5VSB)
24	GND	GND	GND	GND

Table 1.6.1-2 Signal Description for Others in SMD 64-Pin

1.7 General Layout Guidelines

This section provides general layout guideline for high speed signals, PCI Express, USB and Display port.

1.7.1 Impedance

In a high-speed signaling environment, signal trace impedances must be controlled in order to maintain good signal quality across the motherboard. Signal trace impedance is a function of the following three factors:

- Motherboard stack up
- Dielectric constant of the PCB substrate
- Signal trace width and thickness

1.7.2 Crosstalk

The following list of recommendations should be followed to help reduce the crosstalk on the motherboard:

- Do not allow high-speed signals to cross plane splits.
- Reference critical signals to ground planes.
- Do not cut ground planes unless it is absolutely necessary.
- Reduce the length of signals that are routed parallel.
- Provide analog signals with guard shields or guard rings.
- Keep analog signals away from digital signals.

1.7.3 Reference Planes

The high-frequency return path for any signal lies directly beneath the signal on the adjacent layer. Providing a solid plane underneath a signal greatly reduces problems with signal integrity, timing, and EMI because the plane provides a direct return path for that signal. There are two cases where a signal can change its reference plane: crossing a plane split or changing signal layers. If either of these are unavoidable, techniques must be used to minimize the negative impact caused by changing reference planes.

1.7.4 Crossing Plane Splits

When crossing a plane split, a 0.1-µF or 0.01-µF stitching capacitor with a 0402 or smaller body size should be used. Place the stitching capacitors as close as possible to the traces crossing the split, as shown in Figure 1.7-1.

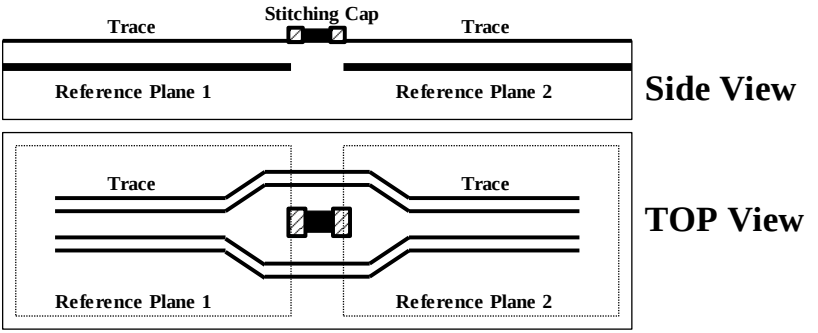


Figure 1.7-1 Trace Crossing Plane Splits

1.7.5 Referencing Different Plane Layers

When signal traces change layers, ground stitching via should be placed amongst the signal via in order to provide a return path. Place the stitching via as close as possible to the signal via, as shown in Figure 1.7-2.

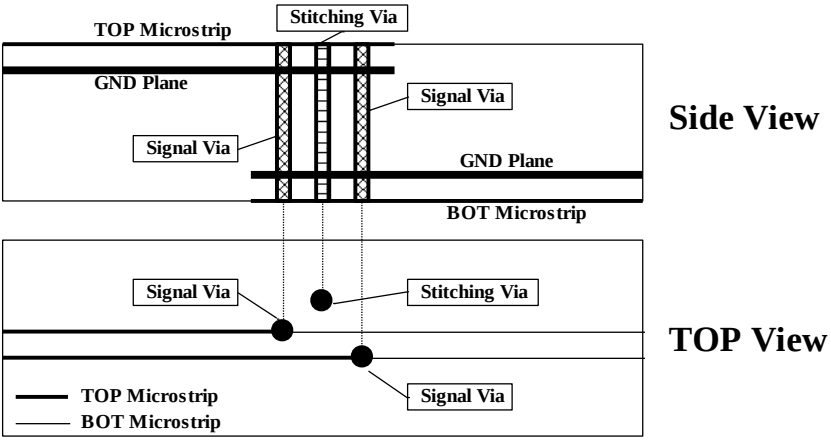
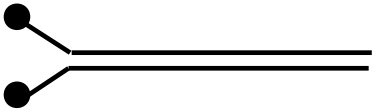


Figure 1.7-2 Ground Stitching Via

1.7.6 Differential pair routing

It is important to maintain routing symmetry between the two signals of a differential pair. Failure to maintain symmetry between the signals of the differential pair will introduce an AC common mode voltage.

Preferred: Symmetrical Routing



Avoid: Non-symmetrical Routing

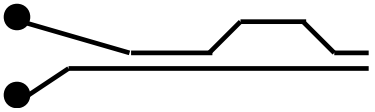


Figure 1.7-3 Symmetrical Routing for differential pair

There is only one lane, and each link will be routed to different devices at varied locations of the board, it is most practical to route the TX signal and the RX signal of that lane next to each other on the same layer.

Differential-Pair length matching should be maintained segment-to-segment. Examples of segments might include breakout areas, route to connect vias, route to connect a connector, and so forth.

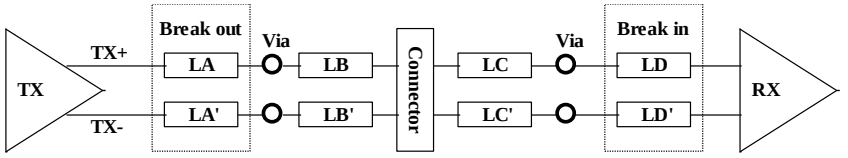


Figure 1.7-4 length matching example

When trace length matching compensation occurs, it should be made as close as possible to the point where the variation occurs, as shown in Figure 1.7-5.

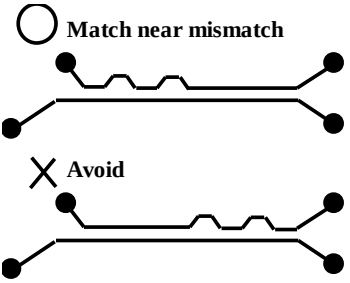


Figure 1.7-5 length matching compensation near mismatch

When serpentining is needed to match lengths, the following guidelines should be maintained. The trace spacing should not become greater than 2 times the original spacing. The length of the increased spacing should not be greater than 3 times the trace width.

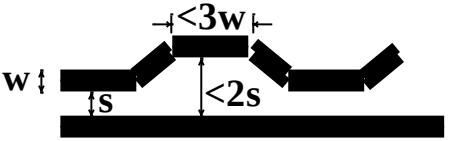


Figure 1.7-6 serpentine rule